SERVICE MANUAL

EQUITY II

BUSINESS COMPUTER

EPSON

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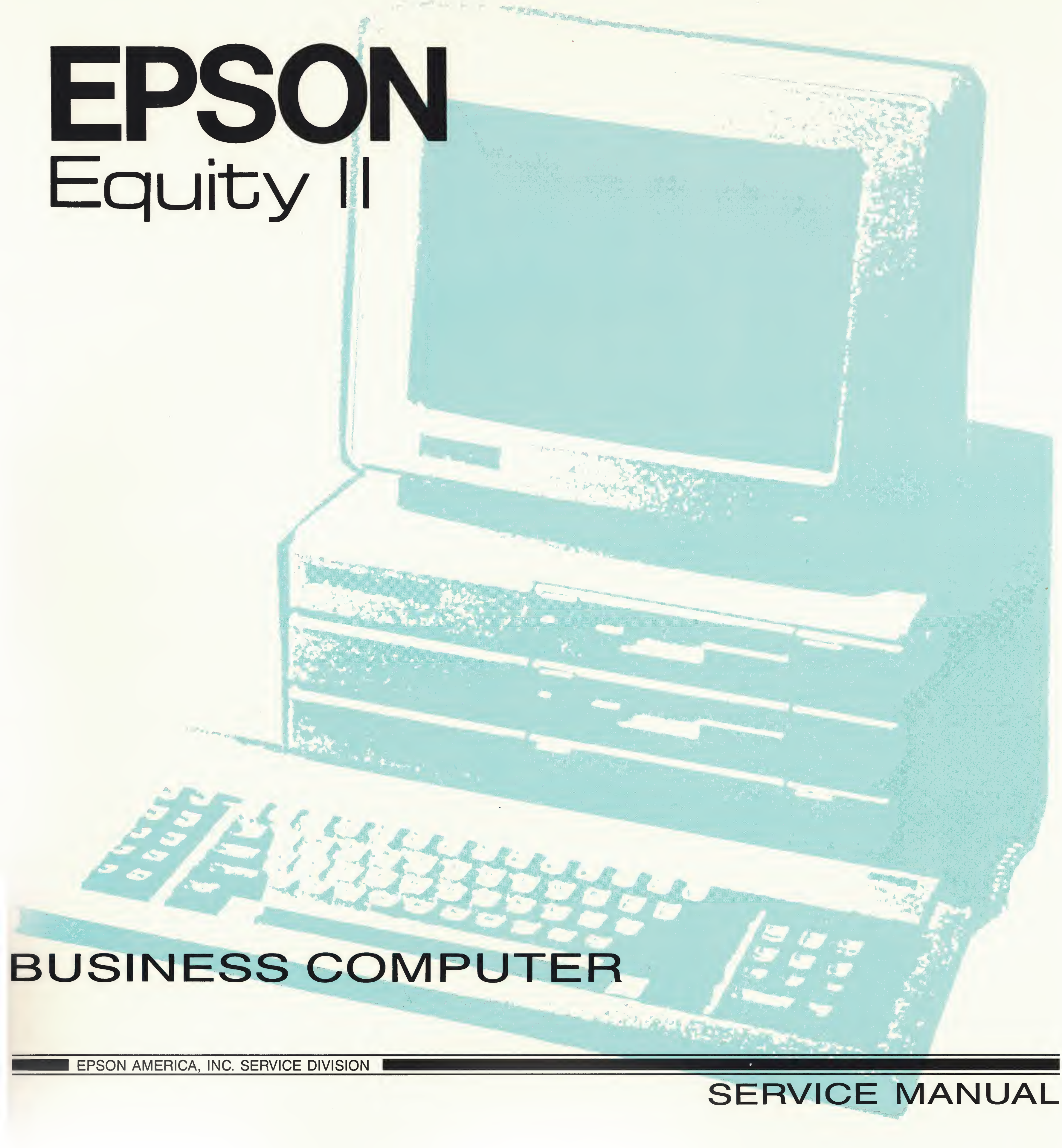

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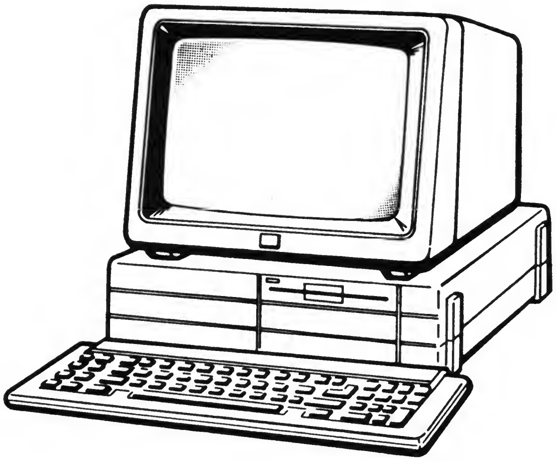

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Nagano, Japan

Y14799900101

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This equipment uses and generates radio frequency energy and if not installed and used properly, that is in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with limits for a Class B computing device in accordance with Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to try to correct the interference by one or more of the following measures:

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DANGER Signals a precaution which, if ignored, could result in serious or fatal personal injury. Great caution should be exercised in performing procedures preceded by DANGER headings.

WARNING Signals a precaution which, if ignored, could result in damage to equipment.

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1. *ALWAYS DISCONNECT THE PRODUCT FROM BOTH THE POWER SOURCE AND PERIPHERAL DEVICES BEFORE PERFORMING ANY MAINTENANCE OR REPAIR PROCEDURE.*
2. *NO WORK SHOULD BE PERFORMED ON THE UNIT BY PERSONS UNFAMILIAR WITH BASIC SAFETY MEASURES AS DICTATED FOR ALL ELECTRONICS TECHNICIANS IN THEIR LINE OF WORK.*
3. *WHEN PERFORMING TESTING AS DICTATED WITHIN THIS MANUAL, DO NOT CONNECT THE UNIT TO A POWER SOURCE UNTIL INSTRUCTED TO DO SO. WHEN THE POWER SUPPLY CABLE MUST BE CONNECTED, USE EXTREME CAUTION IN WORKING ON POWER SUPPLY AND OTHER ELECTRONIC COMPONENTS.*

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REVISION	ISSUE DATE	REVISION PAGE
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PREFACE

This manual describes the theory of operation of the EQUITY II microcomputer system, and includes troubleshooting, repair, and maintenance procedures for serviceing system subassemblies. This text is divided into seven chapters:

CHAPTER 1.	PRODUCT DESCRIPTION --- Describes the features and specifications of the computer, illustrates system components, and lists the logic configuration of the primary circuit boards.
CHAPTER 2.	PRINCIPLES OF OPERATION --- Details the functional organization of the logic circuitry.
CHAPTER 3.	OPTIONS --- Describes option card specifications and the operating principles of the options.
CHAPTER 4.	TROUBLESHOOTING --- Provides instructions for isolating computer malfunctions.
CHAPTER 5.	DISASSEMBLY AND ASSEMBLY --- Describes system disassembly for replacement of malfunctioning subassemblies.
CHAPTER 6.	ADJUSTMENT AND MAINTENANCE --- Lists the necessary adjustments for unit assembly and servicing.
CHAPTER 7.	DIAGRAMS AND REFERNCE MATERIALS --- Describes jumper settings, DIP switch settings, connector pin assignments and I/O port address. This chapter also illustrates IC pin configurations, and provides exploded, circuit board layout, and schematic diagrams for use in conjunction with the text.

Subsequent product modifications will be brought to your attention via Service Bulletins; please revise the text as bulletins are received.

This document is subject to change without notice.

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CHAPTER

1

PRODUCT DESCRIPTION

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1.1 **FEATURES** (Figure 1-1)

The EQUITY II computer system includes two major elements; a main system unit and a keyboard. The EQUITY II's hardware configuration has a high degree of compatibility with the IBM PCs, and most of the IBM PC application software run with the EQUITY II. In addition, the EQUITY II accepts most of the option cards for the IBM PC. A standard system unit includes the microprocessor and one 5-1/4" double-sided, double-density floppy disk drive. A 20M byte hard disk unit or 1.2M byte double-sided, high-density, double track, floppy disk drive is available as an option. The keyboard is attached to the main system unit with a light-weight, coiled cable, designed to combine the familiar typewriter and calculator pad layouts.

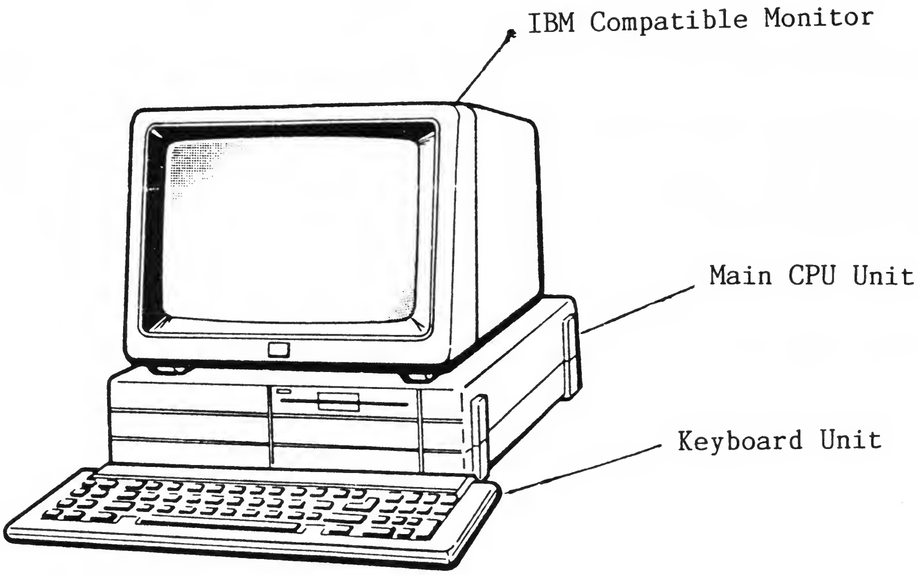

FIGURE 1-1. MAJOR COMPONENTS

1.2 SPECIFICATIONS

The specifications below apply to the entire system; sections following itemize specifications by major subassembly.

POWER SUPPLY

Input Voltage	115 V ± 20% (USA)
Frequency	50/60 Hz
Power Consumption	Approximately 38W (Effective value/No option) Apparent power 220-240 V 2.4A
Inrush Current	32A for 10 ms maximum

INSULATION STRENGTH

100-120 V Units	1 KV for 1 minute between AC power supply and case.
220-240 V Units	1.5 KV for 1 minutes between AC power supply and case.

INSULATION RESISTANCE	50M ohms for 500 VDC minimum

ENVIRONMENTAL CONDITIONS	Operation	Storage
Temperature	5°C to 35°C	-20°C to 65°C
Humidity (no condensation)	20% - 80%	5% - 95%
Maximum Wet Bulb	29 degree: No HDD version 26 degree: HDD version	30 degree
Vibration Resistance (maximum)	0.4G, 5-55 Hz	3G, 5-55 Hz

1.2.1 Main System Unit Specifications

PROCESSOR	uPD70116/V-30
CO-PROCESSOR	8087 (option)
ROM	16KB (two 2764) up to 64KB (two 27256)
RAM	640KB is standard (128KB is provided by Memory Card. RAM for parity check are option.)
MASS MEMORY	5 1/4" FDD or HDD Standard .... one FDD (360KB) Option ...... one FDD (360KB or 1.2MB) or one HDD (10MB or 20MB)
DISPLAY MODE	Monochrome ..... 720 x 350 pixels Character mode ... 80 x 25 chr. 64 KByte Graphic mode ..... 720 x 348 dots 64 KByte Color .... 640 x 200 pixels Character mode ... 80 x 25 chr. 40 x 25 chr. Graphic mode ..... 640 x 200 dots and 320 x 200 dots

Same V-RAM is used at monochrome mode and color mode.

PERIPHERALS	Parallel I/F .... Printer Serial I/F ...... RS-232C (50-56.0Kbps, full duplex, async) Keyboard I/F .....IBM compatible Real time clock...Battery back up
OPTION SLOTS	Five slots IBM option slot pin comapatible
CPU CLOCK	7.16MHz/4.77MHz (Software selectable)
CONTROLABLE EXECUTION SPEED	0 to 7 waits are software-selectable
POWER ON/OFF SOFTWARE CONTROL	
DIMENSIONS (w x d x h)	365 x 376 x 145 mm
WEIGHT	FDD x 1 : 9.1 Kg FDD x 2 : 10.5 Kg FDD x 1, HDD x 1 : 10.9 Kg

1.2.2 Keyboard Specifications

LAYOUT	Closed to IBM PC's
DIMENSIONS (w x d x h)	161.9 x 177.8 x 38.1 mm
WEIGHT	1.37 Kg

1.2.3 SD-521 Floppy Disk Drive Specifications

DRIVE SIZE	5.25 inch drives (two)
RECORDING METHOD	MFM
STORAGE CAPACITY	
Unformatted	500K bytes
Formatted (16 sectors/track)	328K bytes
NUMBER OF TRACKS	80 (40 per side)
TRACK DENSITY	48 TPI
RECORDING DENSITY (side 1, track 39)	5876 BPI (double density)
TRACK RADIUS	
Innermost Track (TK 39)	Side 0 : 36.25 mm Side 1 : 34.40 mm
Outermost Track (TK 00)	Side 0 : 57.15 mm Side 1 : 55.03 mm
TRANSFER RATE	250K bits per second
AVERAGE ROTATIONAL DELAY	100 msec
ACCESS TIME	
Track-to-Track	6 msec
Average	97 msec
Setting Time	15 mesc
READ/WRITE HEAD	
Type	Tunnel erase head with gimble support
Positioning Sytem	Stepper motor
DRIVE MOTOR	Direct drive spindle motor
Start-up Time	0.5 sec or less
Speed	300 rpm
SENSORS	Index, track 00, and write protect
POWER REQUIREMENT	
+12 V Read Current	0.3A typical, 1.4A maximum 250 mVpp maximum ripple
+ 5 V Read/Write Current	0.2A typical, 0.25A maximum 100 mVpp maximum ripple
POWER DISSIPATION	4.6 W typical during operation
DIMENSIONS (w x d x h)	146 x 195.5 x 41 mm (5.7 x 7.7 x 1.6 inches)
WEIGHT	1.3 Kg (3.0 lbs)

1.2.4 SD-581L Floppy Disk Drive Specifications

ITEM	MODE	HIGH DENSITY MODE	STANDARD DENSITY MODE
Strorage capacity	Unformatted	1604 KB	1000 KB
	Formatted	1025 KB (26 sectors/track)	656 KB (16 sectors/track)
Recording density (MFM)		9646 BPI (track 76, side 1)	5922 BPI (track 79, side 1)
Data transfer rate (MFM)		500 K bits/sec	250 K bits/sec
Average rotational delay		83 msec	100 msec
Access time	Track to track	3 msec	
	Average	93 msec	
	Setting time	15 msec	
Head load time		50 msec	
Track density		96 TPI	
Number of tracks		154	160
Direct drive spindle motor	Start-up time	1.0 sec	
	Rotational Speed	360 RPM	300 RPM
Power Supply	+12 V (+5%)	0.4A (TYP) 1.5A (MAX) (motor start-up)	
	+5 V (+5%)	0.5A (TYP) 0.8A (MAX)	
	Start-up time	10 msec (MAX) (12 V and 5 V)	
Power		7.3 W (TYP)	
Mechanical dimensions	Wideth	146.0 mm (5.7 inch)	
	Death	195.5 mm (7.7 inch)	
	Height	41.0 mm (1.6 inch)	
Weight		1.4 Kg (3.08 lbs)	
Reliability	MTBF	10000 POH	
	MTTR	0.5 hour	
	Soft error rate	1 per 10 bits read	
	Hard error rate	1 per 10 bits read	
	Seek error rate	1 per 10 seeks	

1.3 **HARDWARE CONFIGURATION** (Figure 1-2)

The EQUITY II computer is composed of the main CPU unit, comprised of the power supply, controller, and graphics boards; the keyboard; one or two floppy disk drives; and one hard disk drive.

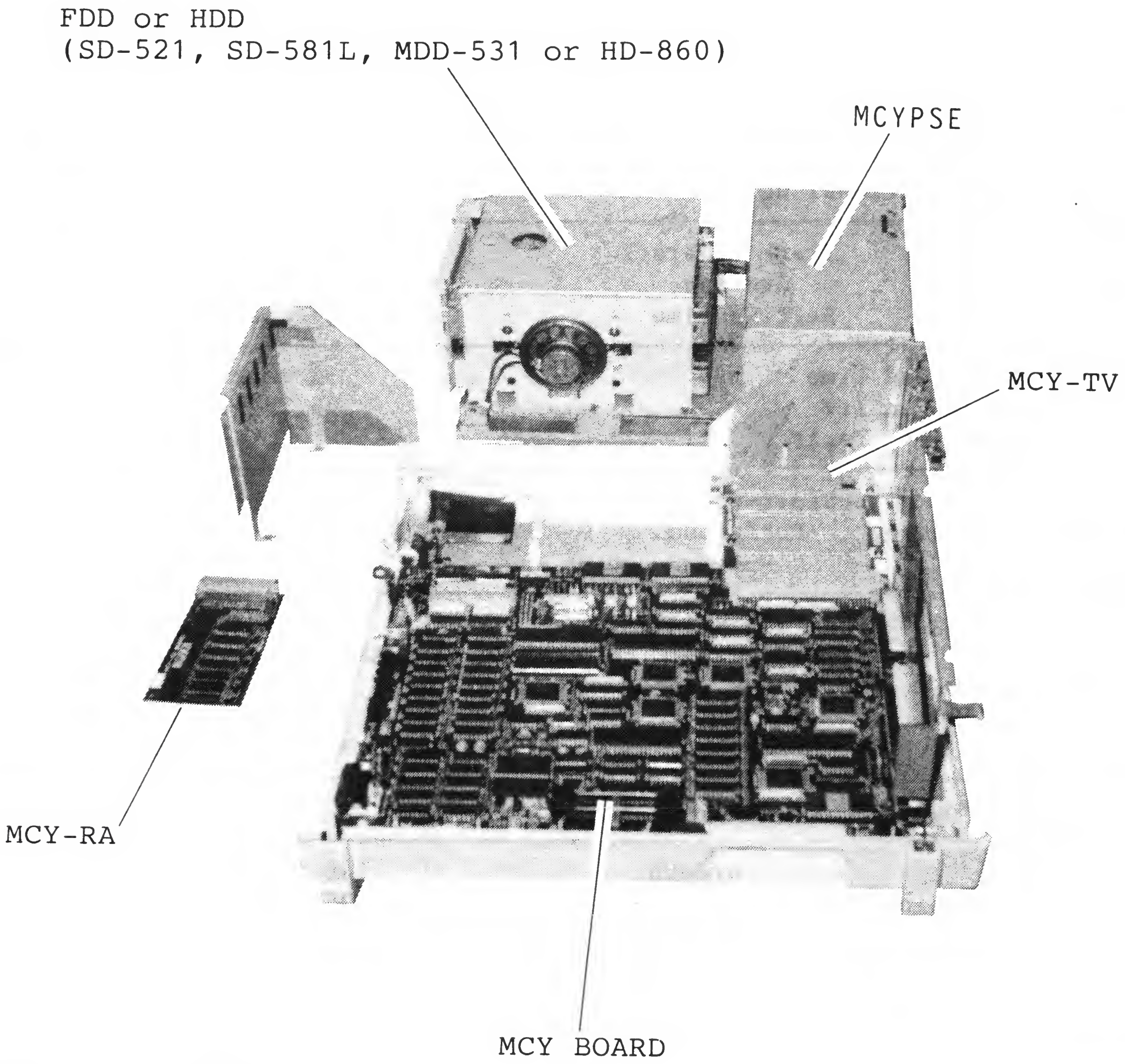

FIGURE 1-2. COMPONENT LOCATIONS

1.3.1 **Main System Unit Components** (Figures 1-3 through 1-7)

The main system unit houses the MCYPSE power supply unit, which includes the switching regulator; the MCY control board, which includes the uPD70116/V-30 processors and related logic components. The logic component relationship is diagrammed in Figure 1-3. Figure 1-4 and Table 1-1 show the layout and functions of the MCY board components. Figure 1-5 and Table 1-2 show the MCYPSE power unit. The main system unit also houses one or two floppy disk drives or hard disk drives; however, the disk drives are discussed separately throughout the text.

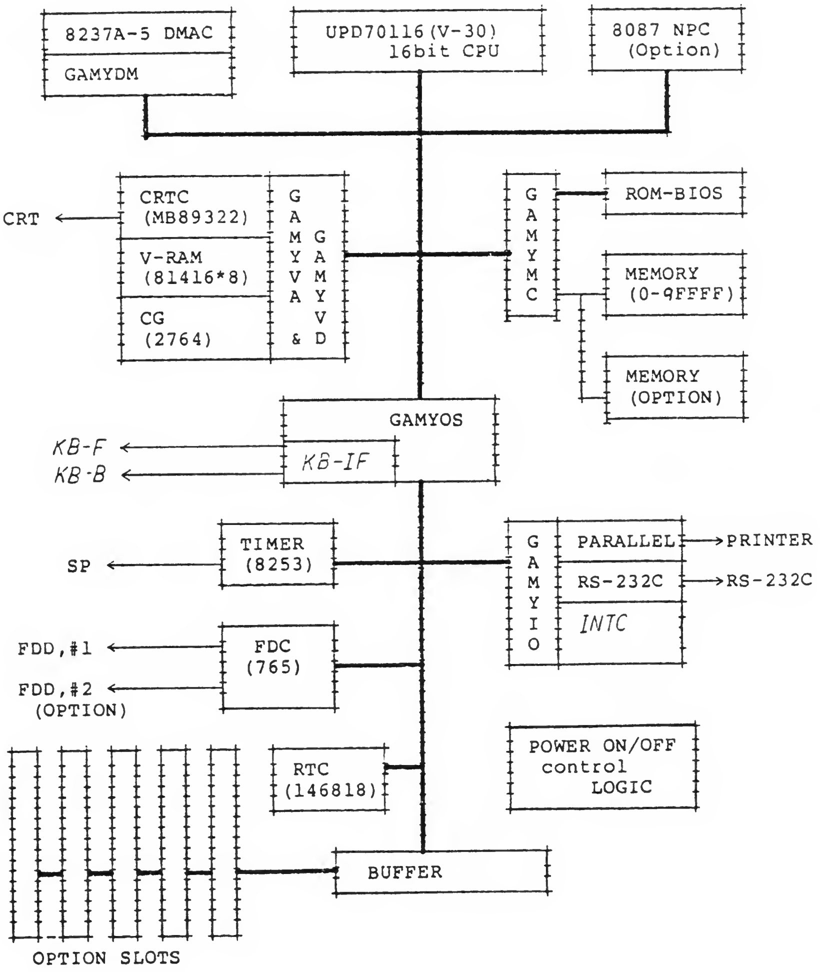

FIGURE 1-3. LOGIC BLOCK DIAGRAM

TABLE 1-1. MCY BOARD COMPONENT DESCRIPTION

NAME	MODEL	IC LOCATION	Q'TY	FUNCTION
CPU's	uPD70116 8087	1Q 1P	1 1	16 bit CPU Co-processor
GAMYMC	E01064EA	7L	1	Gate array for the memory controller
GAMYDM	E01063EA	4N	1	Gate array for the DMA controller
GAMYVD GAMYVA	E02052EA E02051EA	2D	1	Gate array for the video controller
GAMYOS	E01062EA	3N	1	Gate array to control for the option slot.
GAMYIO	E01061EA	4K	1	Gate array for the I/O controller.
DMA Controller	8237	4Q	1	Controls direct memory access
Read Time Clock	146818	7C	1	Generates date and time.
CRT Controller	MB89322	2H	1	Controls to display the monitor
Main Memory	MB81256-10	8H 8J-8N 8P,8Q 9H 9J-9N 9P,9Q	16	256K bit dynamic RAM.
Video Memory	MB81416-10	3C-3F 3H,3J 2K,3L	1	Used for Video memory
Character Generator ROM	2764	1B	1	Used for character generator ROM.
BIOS ROM	2764	4U	1	Used for BIOS ROM.
BIOS ROM	2764	5U	1	Used for BIOS ROM.

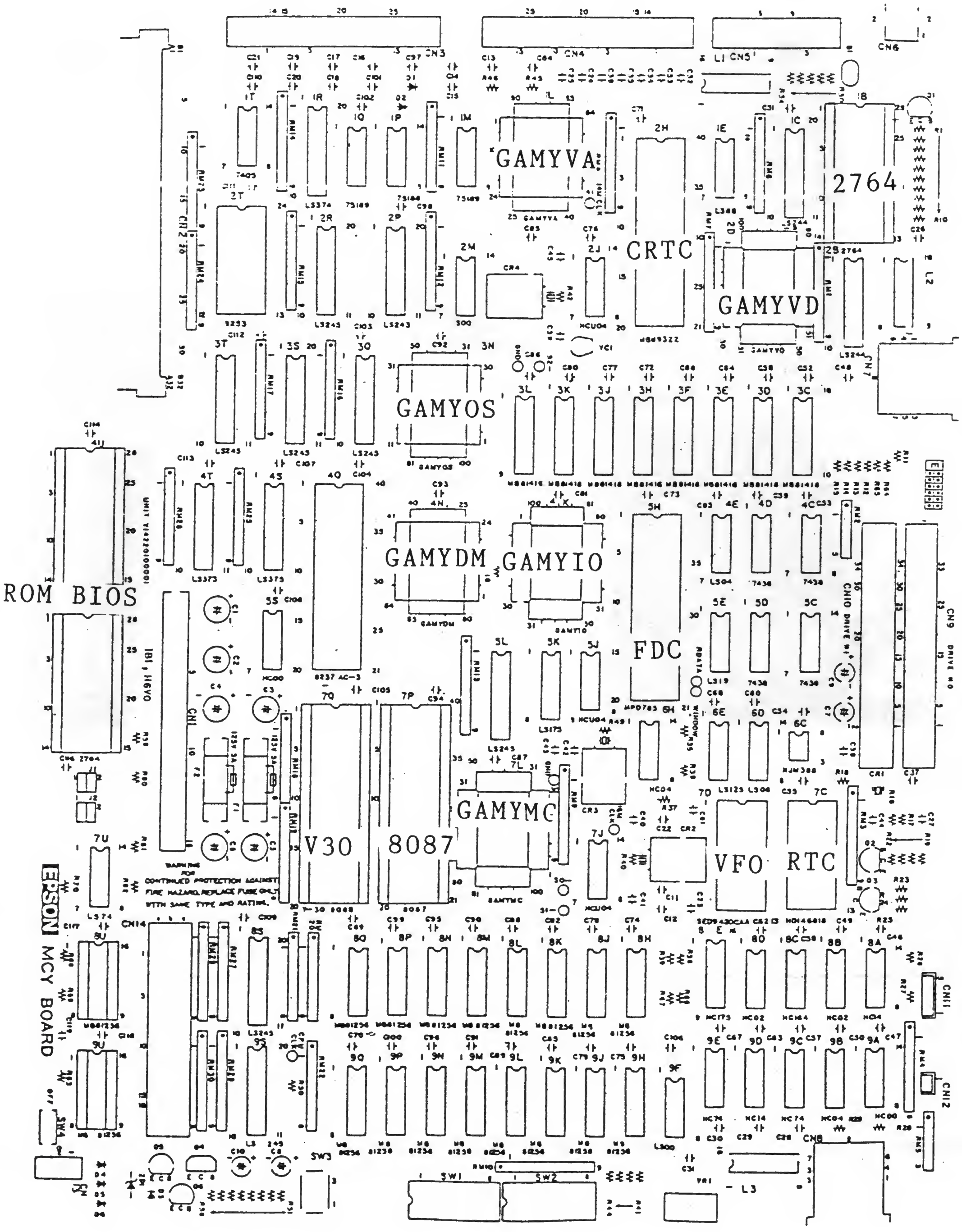

FIGURE 1-4. MCY CONTROL BOARD

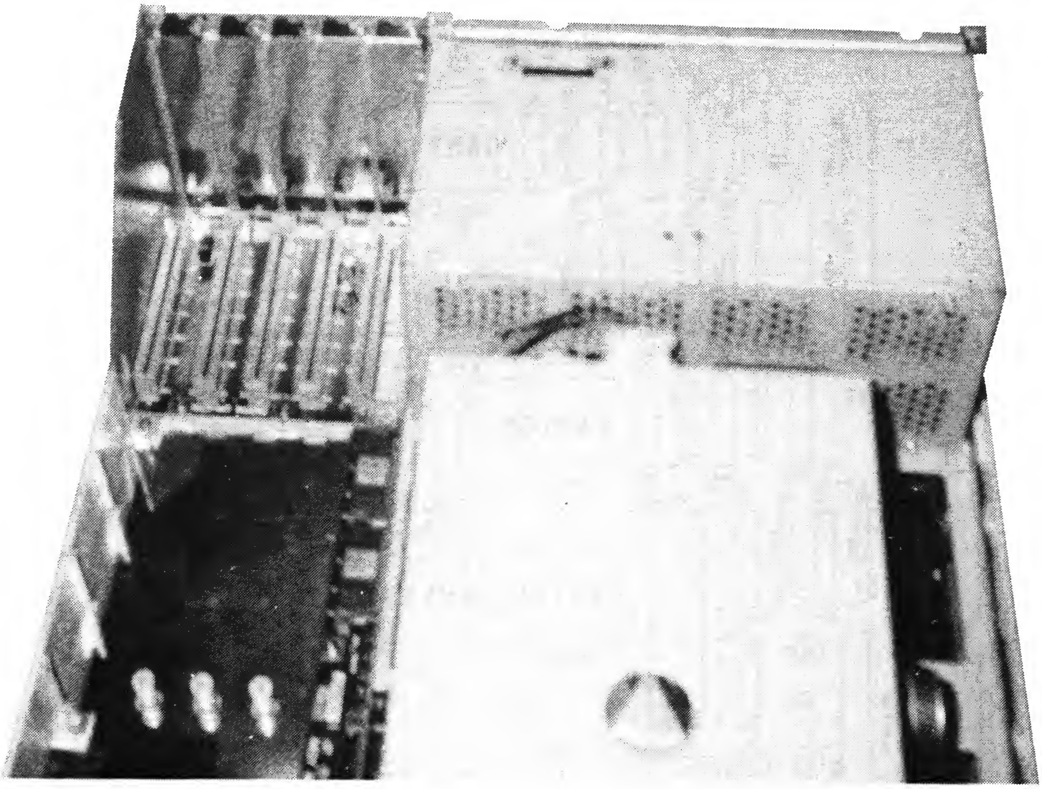

FIGURE 1-5. MCYPSE UNIT

TABLE 1-2. MCYPSE UNIT OUTPUT VOLTAGE

OUTPUT VOLTAGE	VOLTAGE LIMITS	LOAD CURRENT CAPACITY
+5	5.0 V ± 5%	Min.1.0A - Max.7.5A
+12	12.0 V ± 5%	Min.0.32A - Max.4.7A
-5	-5.0 V ± 10%	Max.0.3A
-12	-12.0 V ± 10%	Max.0.3A

1.3.2 Floppy Disk Drive Components (Figures 1-6 and 1-7)

Two kinds of floppy disk drives are available in the system CPU unit, Figure 1-6 shows the SD-521 floppy disk drive, which performs double-sides, double density recording (40 tracks per side). A brushless, direct-drive spindle motor ro-tates the disk at 300 rpms; a steper motor and steel band positioner move the head rapidly (3 ms access time) and with a high reliability. The other floppy disk drive, the SD-581L, is shown is Figure 1-7. This drive performs double-sided, high-density, double track recording, and has 1.2M byte disk capacity.

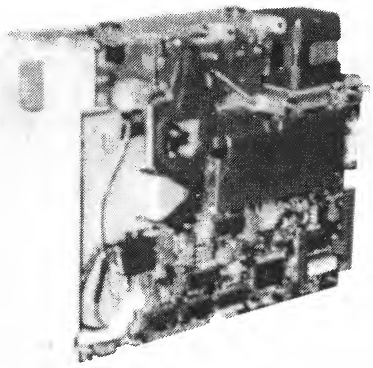

FIGURE 1-6. SD-521 FLOPPY DISK DRIVE

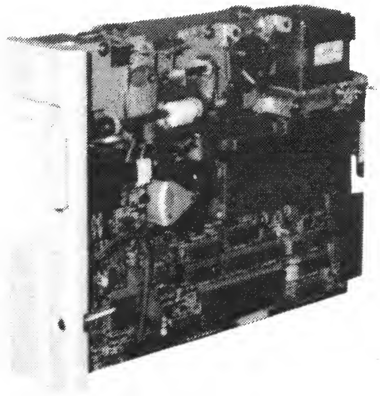

FIGURE 1-7. SD-581L FLOPPY DISK DRIVE

1.3.3 Keyboard Components (Figure 1-8)

The keyboard is attached to the main system unit with a light-weight, coiled cable. The keyboard layout is closer to the "Standard" or typewriter-like keyboard. The keyboard interface is functionally compatible with IBM PC's.

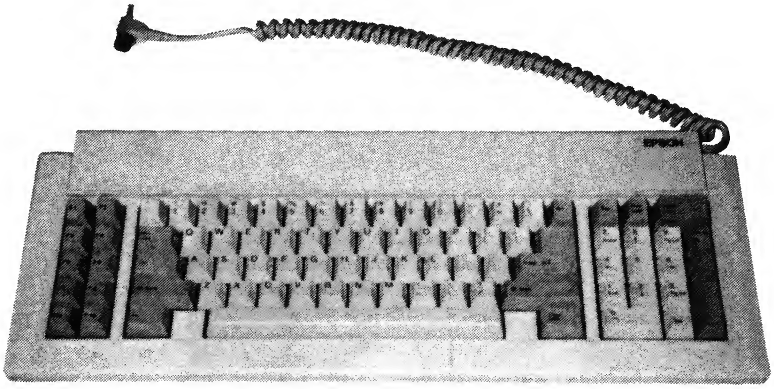

FIGURE 1-8. KEYBOARD COMPONENT

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2

PRINCIPLES OF OPERATION

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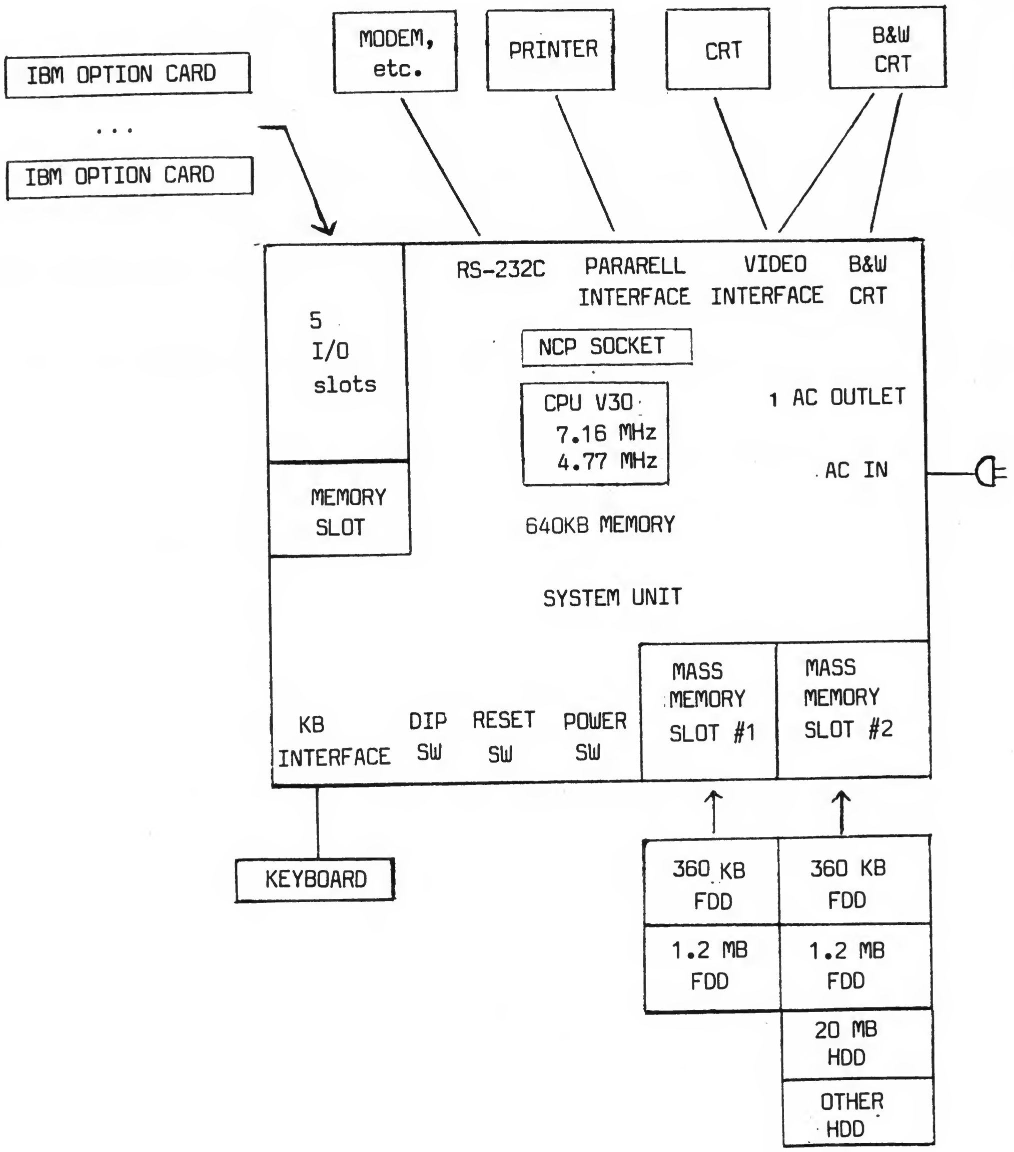
2-17 Power Supply Specification 2-64

2.1 SYSTEM OVERVIEW (Figure 2-1)

Figures 2-1 shows the interconnection of the main CPU unit, floppy disk drives, the keyboard, and the monitor. Pin assignments for each connector are detailed in Chapter 7.



B

FIGURE 2-1. SYSTEM CONFIGURATION BLOCK DIAGRAM

2.2 MCY BOARD OPERATION

2.2.1 System Control Signal Generator Circuit

2.2.1.1 Clock Generator Circuit (Figures 2-2 and 2-3)

The GAMYMC generates the system clock. Two system clock modes - 4.77 MHz and 7.16 MHz can be available on this system. The clock selection is executed by software. At the power on and the reset, a 4.77 MHz is set. The clock speed is indicated by the LED color on the front panel.

TABLE 2-1. LED COLOR INDICATOR

CPU CLOCK	LED COLOR
4.77 MHz	RED
7.16 MHz	GREEN

Figure 2-2 diagrams the clock generator circuit.

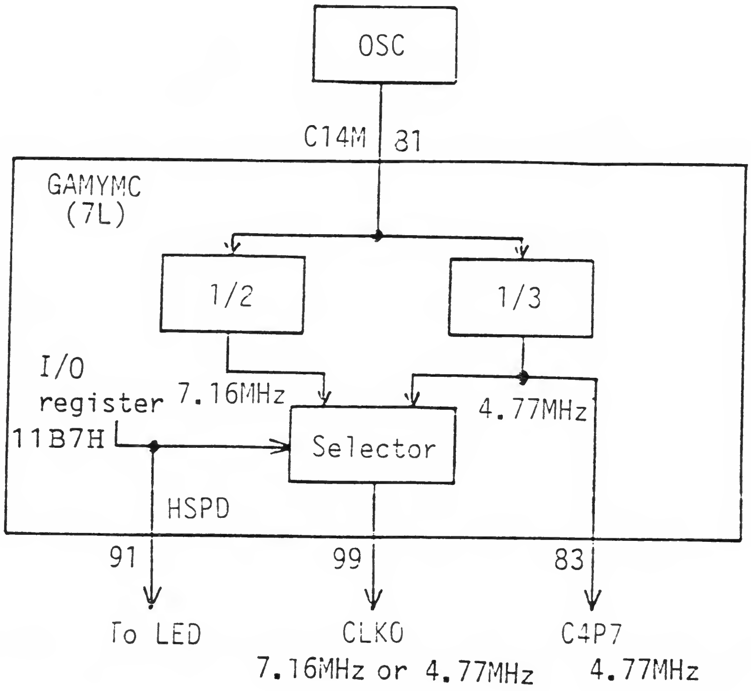
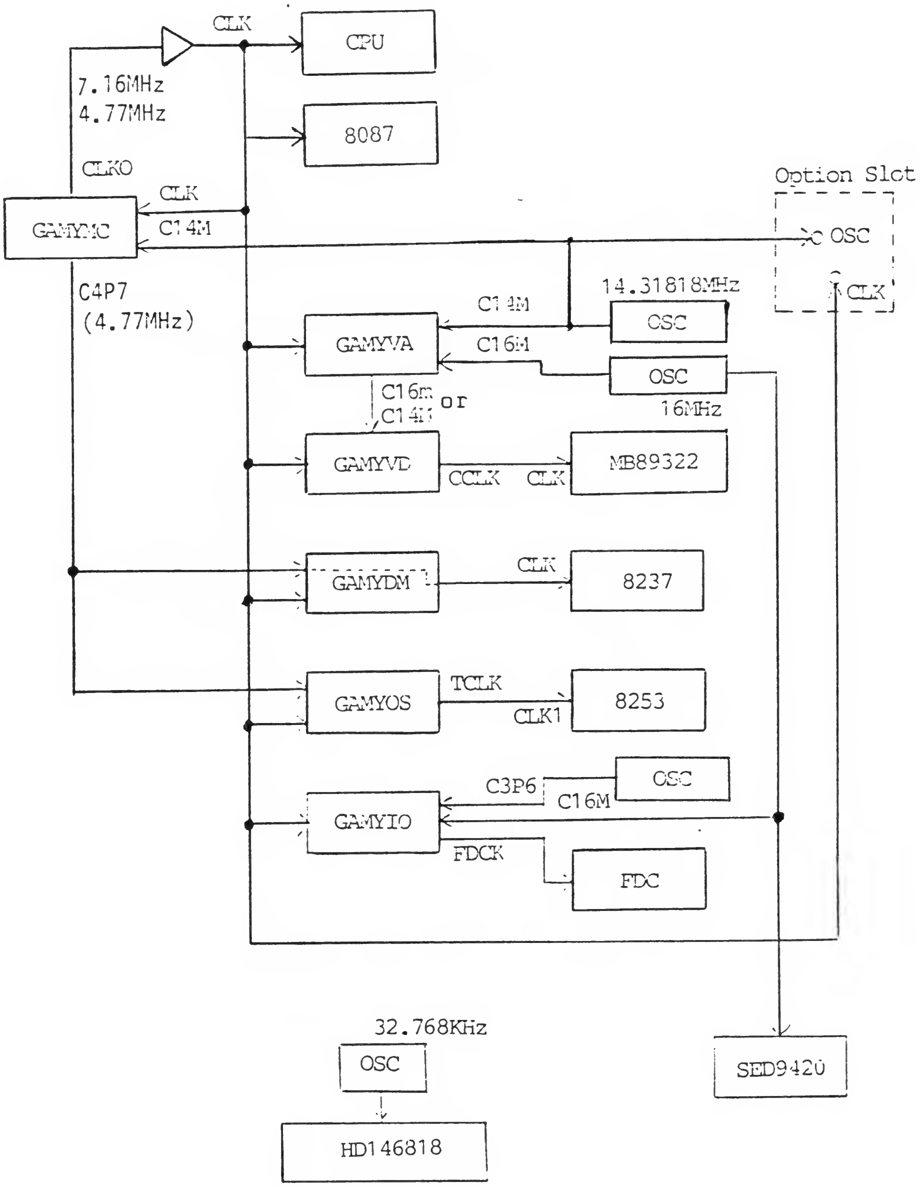


FIGURE 2-2. CLOCK GENERATOR CIRCUIT

Figure 2-3 shows the connections between the clock generator circuit and each device.



B

FIGURE 2-3. CONNECTIONS OF CLOCK SIGNALS

2.2.1.2 Reset Circuit (Figure 2-4)

The reset signal is provided with two signal inputs; the power down detect signal and the reset signal controlled by the reset button. Figure 2-4 shows the reset signal supply circuit on the MCY main control board.

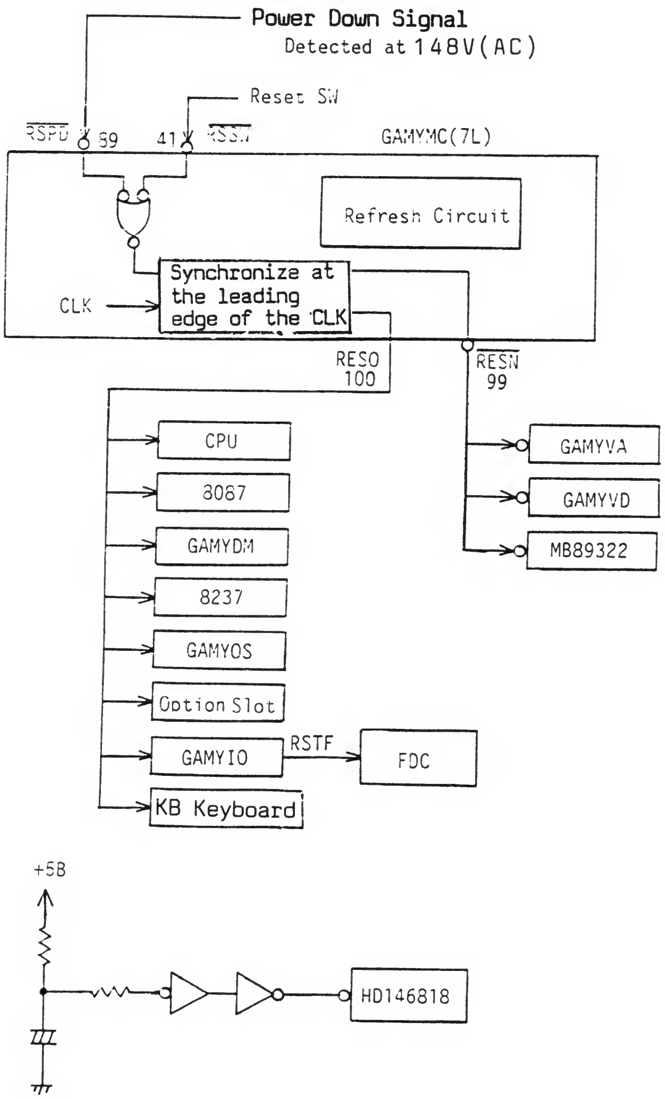
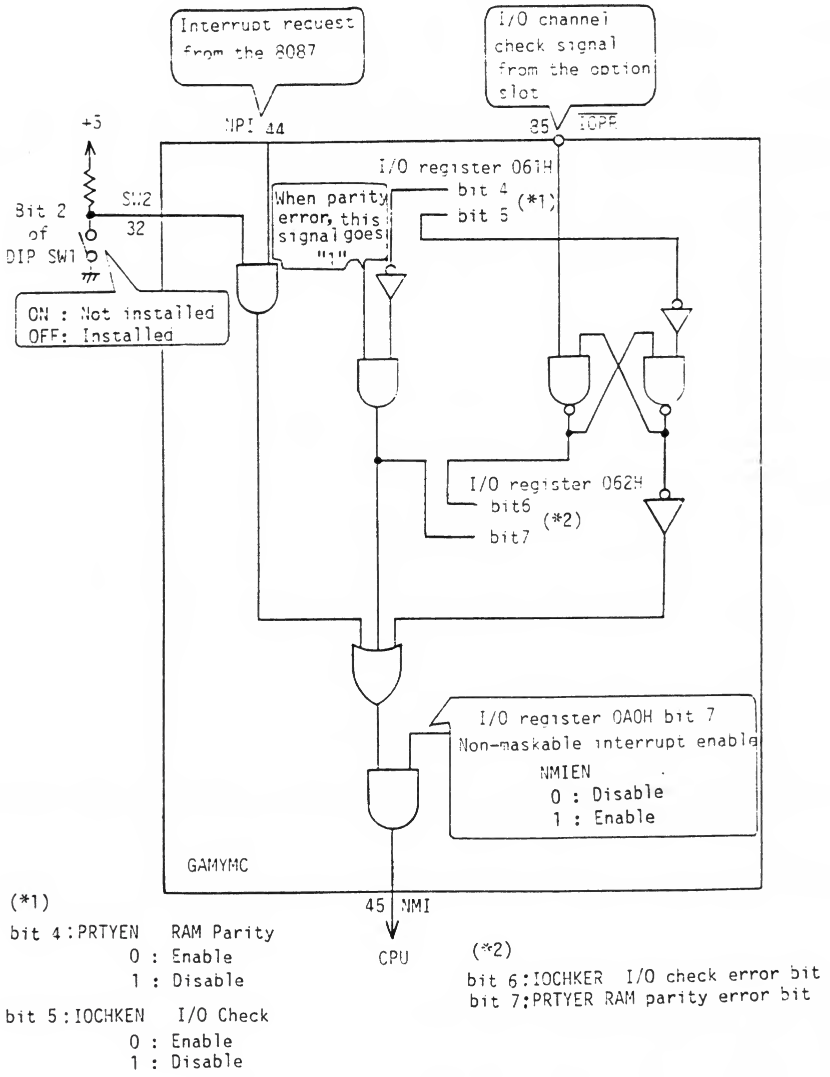


FIGURE 2-4. RESET SIGNAL SUPPLY CIRCUIT

2.2.1.3 NMI Control Circuit (Figure 2-5)

The GAMYMC also employs the nonmaskable interrupt control. The NMI signal is supplied with three signal inputs - bit 2 of the DIP SE2, the interrupt request signal from the 8087 and the I/O channel check signal from the option slot.



(*1)

bit 4 :PRTYEN RAM Parity
0 : Enable
1 : Disable

bit 5 :IOCHKEN I/O Check
0 : Enable
1 : Disable

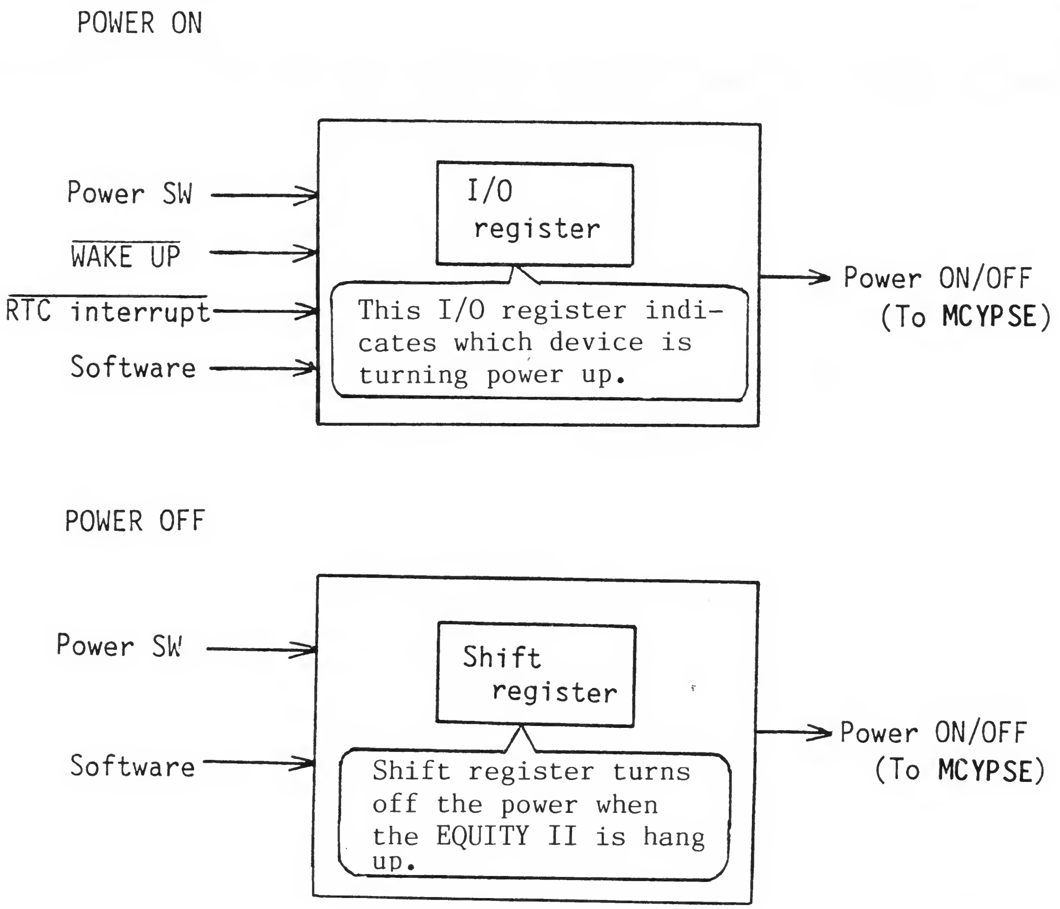
(*2)

bit 6 :IOCHKER I/O check error bit
bit 7 :PRTYER RAM parity error bit

FIGURE 2-5. NMI CONTROL CIRCUIT

2.2.1.4 Power On/Off Control Circuit (Figures 2-6 through 2-13)

Figure 2-6 shows the relationship between input and output signals in the power on/off control circuit.



B

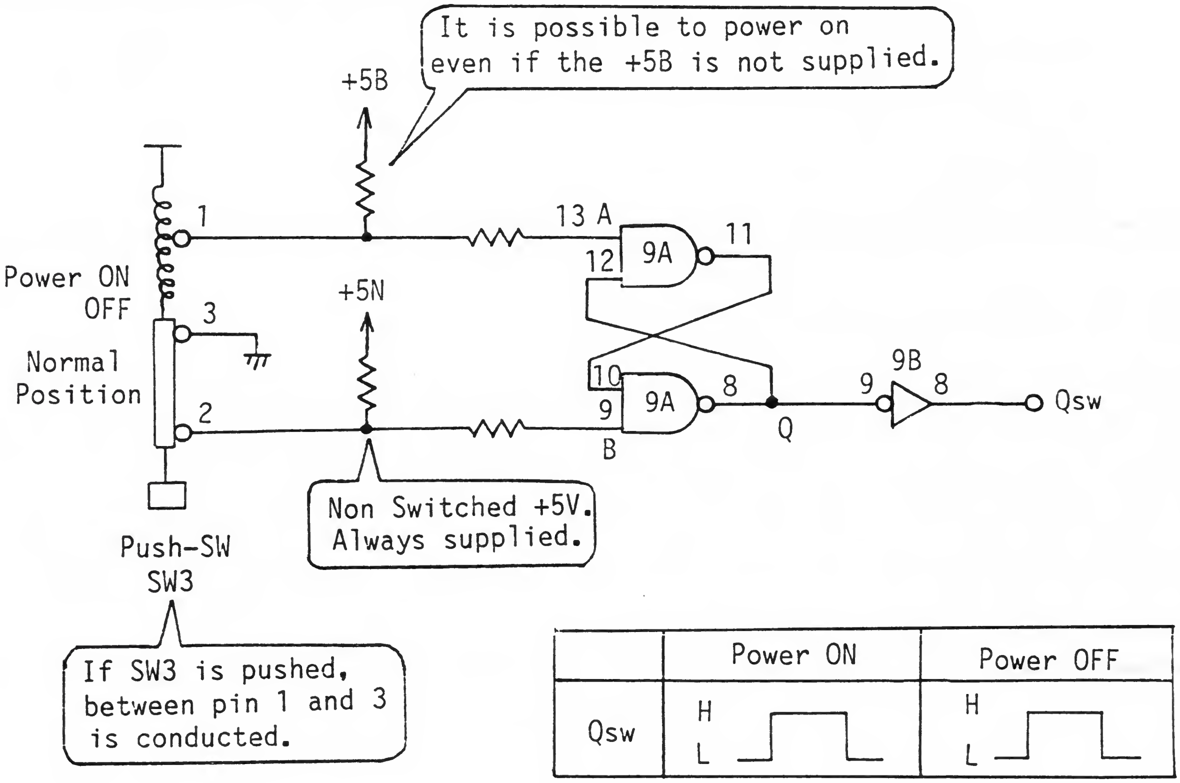
FIGURE 2-6. POWER ON/OFF CONTROL CIRCUIT

The power on/off control circuit is divided into the following six circuits by function:

1. Switch circuit
2. Power on/off signal output circuit
3. Power on signal generator circuit
4. Power off signal generator circuit
5. Power on/off control circuit by software
6. Power on device detector circuit

Switch Circuit

An unlocked POWER switch is located on the front panel of the EQUITY II. At the normal position, this switch connects pin 2 and pin 3 of the SW3, setting pin 9 of IC 9A to low. When the POWER switch is pressed, it connects pin 1 to pin 3 of the SW3. When the switch is released, pin 2 of the SW3 is connected to pin 3. Figure 2-7 shows the POWER switch circuit.



It is possible to power on even if the +5B is not supplied.

Non Switched +5V. Always supplied.

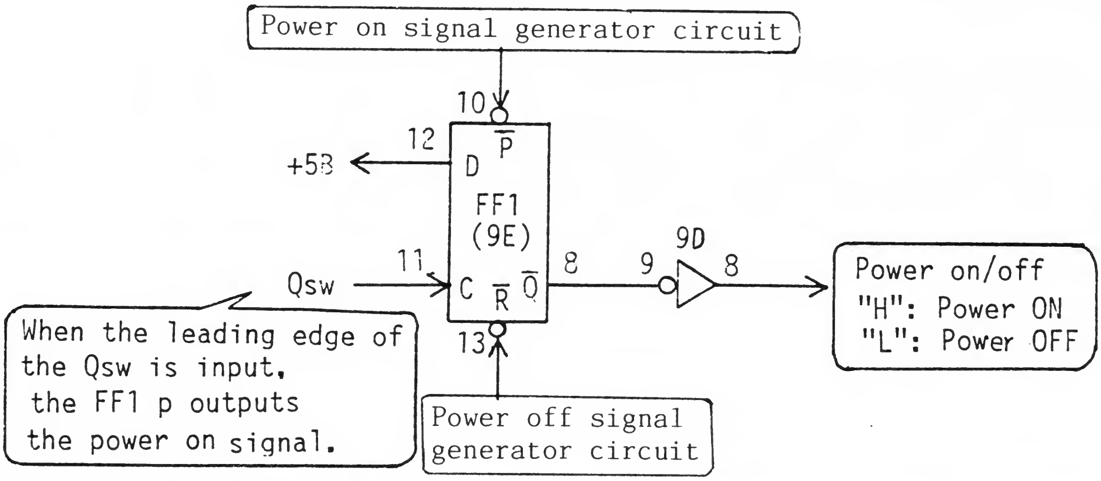
If SW3 is pushed, between pin 1 and 3 is conducted.

FIGURE 2-7. POWER SWITCH CIRCUIT

Power On/Off Signal Output Circuit

Figure 2-8 shows the power on/off signal output circuit. The FF1 (IC 9E) outputs the power on/off signal to the MCYPSE power supply unit. The Qsw signal is input into the clock terminal (pin 11). When this terminal receives a leading edge of the Qsw signal, the Q terminal outputs a low signal, supplying a high signal to the power supply unit. At this time, the manual power-on operation is performed.

A low active power-on signal is supplied at the preset terminal (pin 10) of the FF1. This signal becomes active through power-on of the modem or by the alarm function of the RTC, which turns on the power for the system unit. A low active power-off signal is supplied at the reset terminal (pin 13) of the FF1. This signal becomes active when the power is turned off manually or when the power for software is turned off (bit 7, 11B8H, of the I/O register is turned off).


Power on signal generator circuit
10
12
+5B
D
P̄
FF1
(9E)
11
Qsw
C
R̄
Q̄
8
9
9D
8
13
Power on/off
"H": Power ON
"L": Power OFF
When the leading edge of the Qsw is input, the FF1 p outputs the power on signal.
Power off signal generator circuit

B

FIGURE 2-8. POWER ON/OFF SIGNAL OUTPUT CIRCUIT

Power On Signal Generator Circuit

Figure 2-9 shows the system power-on signal generator circuit. An output signal of this circuit is supplied to the P terminal of the FF1 (IC 9E). When this signal is low, the power is turned on in the system unit. The power-on operation by software is performed either by the alarm function of the RTC or by the WAKE-UP signal supplied from the modem. An interrupt signal is supplied from the RTC to pin 9 of IC 8D. This signal becomes active by the alarm interrupt function of the RTC. The power-on signal is input from the modem to pin 8 of IC 8D through the option slot so that the outside circuit can turn on the power for the system unit.

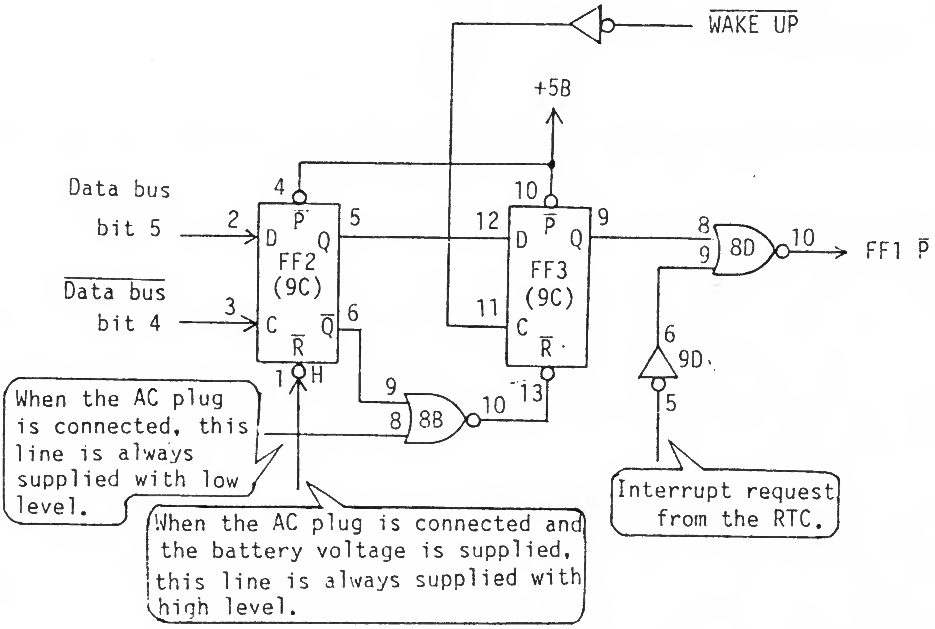
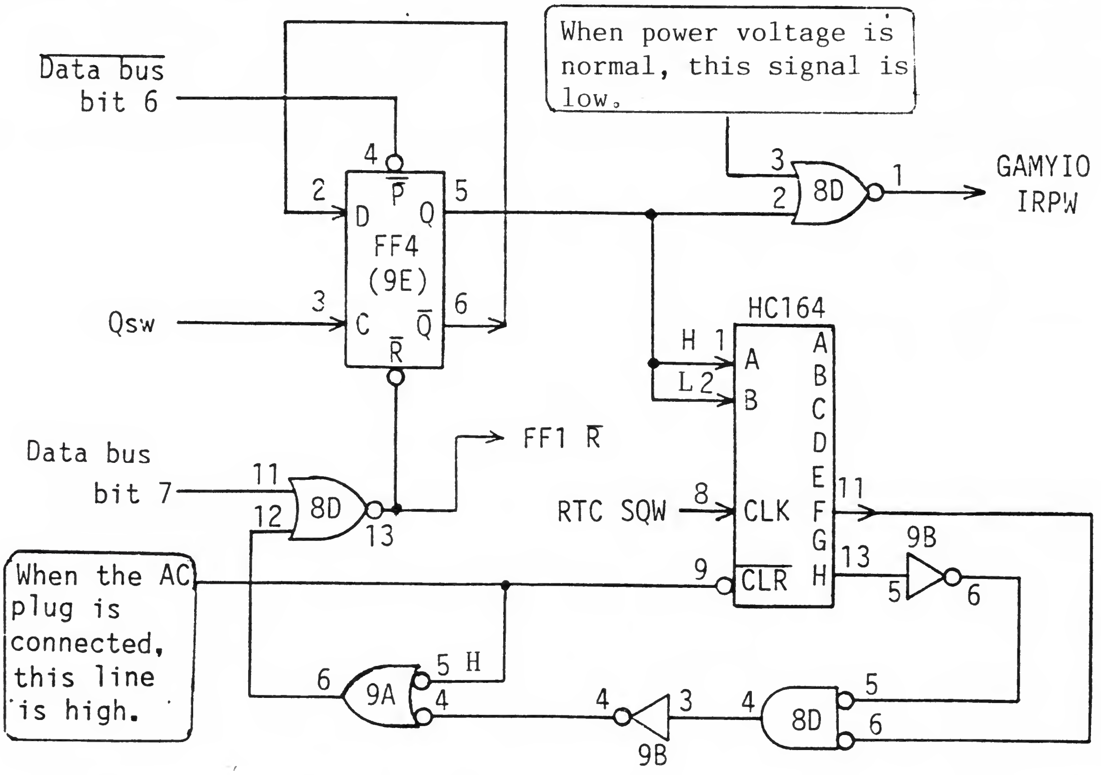

WAKE UP
+5B
Data bus bit 5
Data bus bit 4
4
2
3
D
P̄
Q
FF2
(9C)
C
R̄
Q̄
5
6
1
H
10
12
11
D
P̄
Q
FF3
(9C)
C
R̄
9
13
9
8
8B
10
8
9
8D
10
FF1 P̄
6
9D
5
When the AC plug is connected, this line is always supplied with low level.
When the AC plug is connected and the battery voltage is supplied, this line is always supplied with high level.
Interrupt request from the RTC.

FIGURE 2-9. POWER ON SIGNAL GENERATOR CIRCUIT

Power Off Signal Generator Circuit

As shown in Figure 2-10, bit 7 of the I/O register (11B8H) generates the power-off signal to the R terminal of the FF1. The shift register HC164 (IC 8C) deals with the interrupt due to the power-off, and shifts the time for processing the interruption operation. Figure 2-11 shows the shift register timing diagram.



When power voltage is normal, this signal is low.

When the AC plug is connected, this line is high.

FIGURE 2-10. POWER OFF SIGNAL GENERATOR CIRCUIT

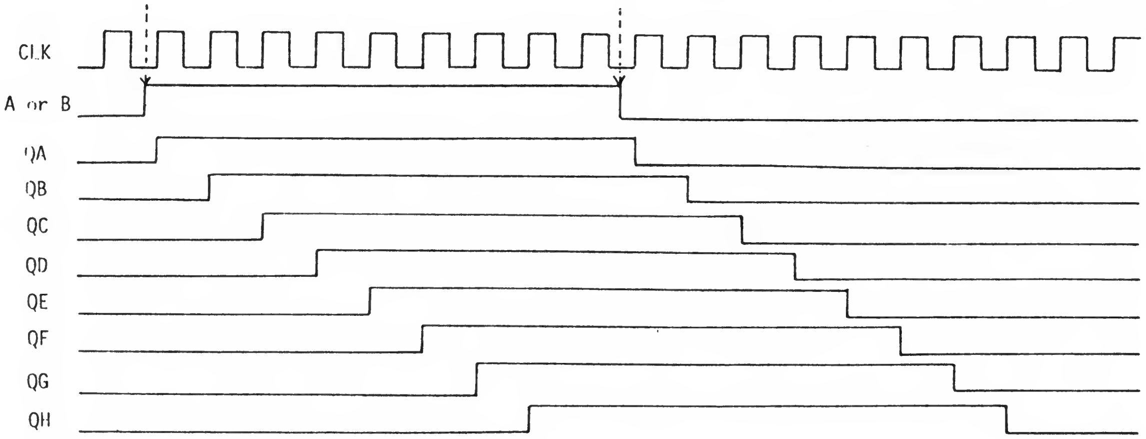
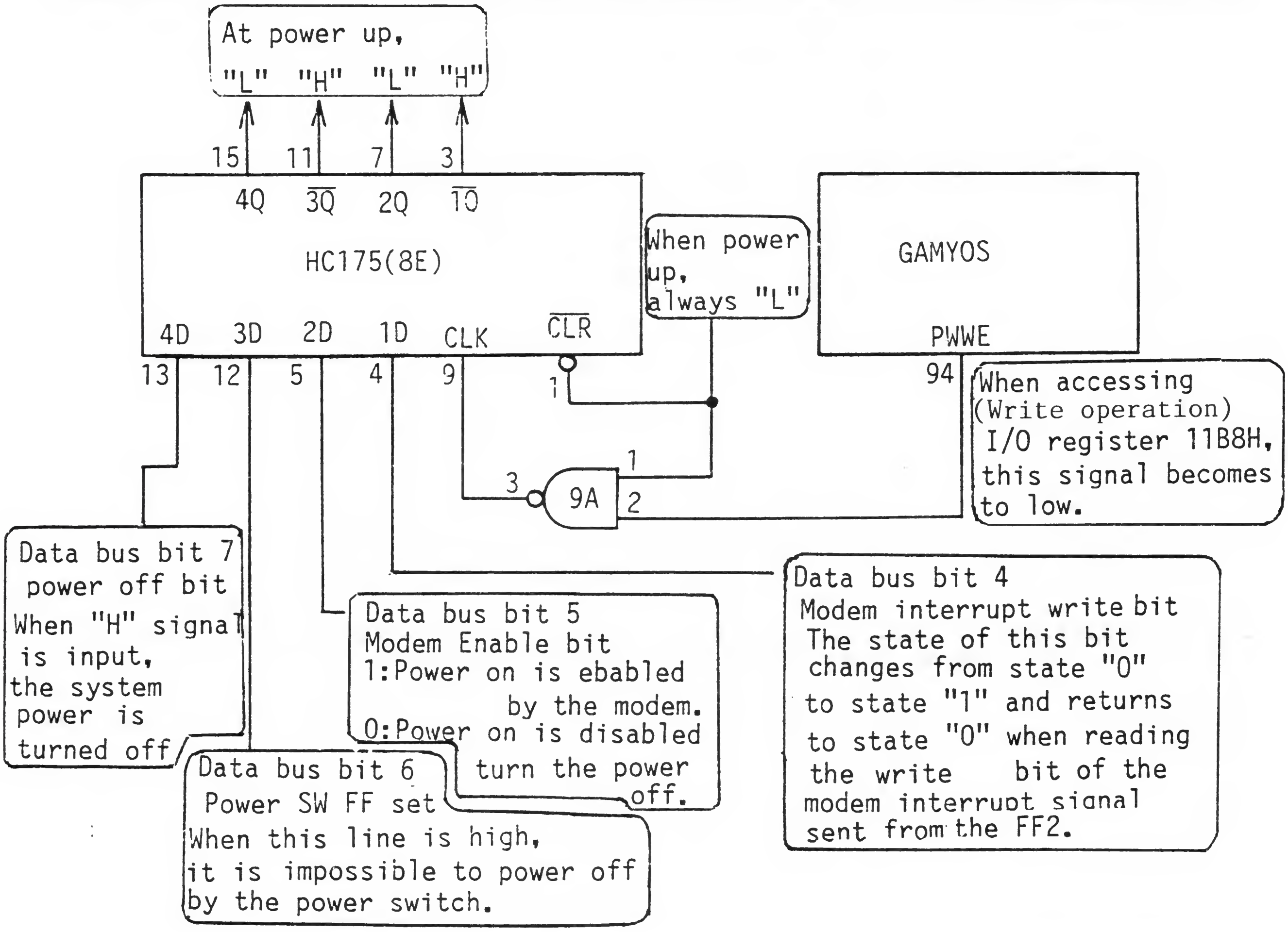


FIGURE 2-11. SHIFT REGISTER TIMING DIAGRAM

Power On/Off Control Circuit by Software

Figure 2-12 shows the power on/off control circuit by software. Data bus bit 7 is input to pin 13 of IC 8E. When the input signal is high, the power for the system unit is turned off. Data bus bit 6 is input to pin 12 of IC8. When this line is high, the POWER switch does not turn the power off. Data bus bit 5 (modem enable bit) enters into pin 5 of IC 8E in the two states- state 1 and state 0. State 1 enables power-on by the modem, and state 0 disables it. Data bus bit 4 (modem interrupt write bit) is brought to pin 4 of IC 8E. When this bit reads the setting of the modem interrupt write bit sent from the FF2, the bit operation changes from state "0" to state "1" and returns to state "0".



B

FIGURE 2-12. POWER ON/OFF CONTROL CIRCUIT BY SOFTWARE

Power On Device Detector Circuit

Figure 2-13 shows the power-on device detector circuit. Pin 13 of IC 8B becomes low when the power is turned on by the WAKE-UP signal sent from the modem. This pin becomes high when the system is turned on by the alarm function of the RTC. If the system is turned on by the POWER switch, pin 1 of IC 8B becomes low. These output signals from the IC 8B are sent to the GAMYOS.

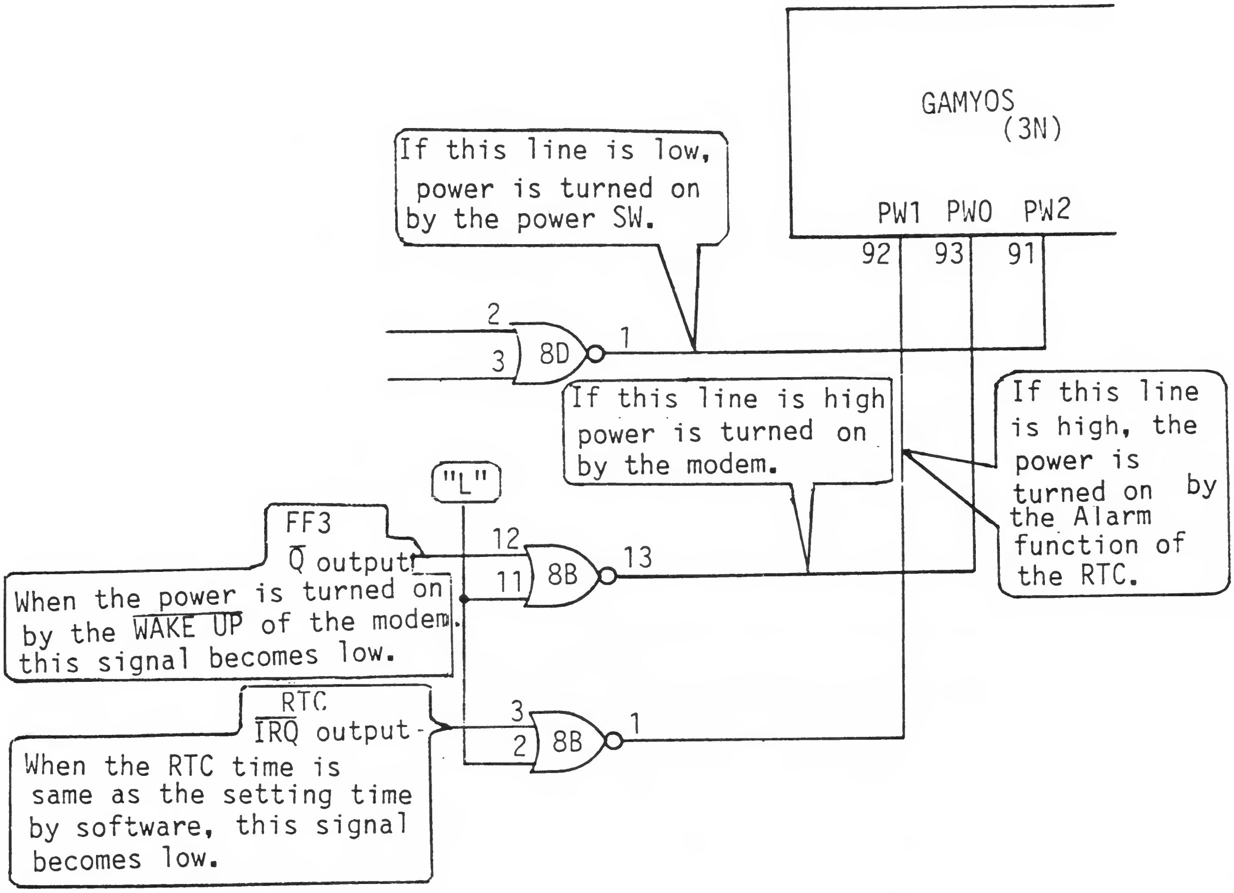

GAMYOS
(3N)
PW1 PW0 PW2
92 93 91
If this line is low, power is turned on by the power SW.
2
3
8D
1
If this line is high power is turned on by the modem.
If this line is high, the power is turned on by the Alarm function of the RTC.
"L"
FF3
$\overline{Q}$ output
When the power is turned on by the $\overline{\text{WAKE UP}}$ of the modem, this signal becomes low.
12
11
8B
13
RTC
$\overline{\text{IRQ}}$ output
When the RTC time is same as the setting time by software, this signal becomes low.
3
2
8B
1

FIGURE 2-13. POWER ON DEVICE DETECTOR CIRCUIT

Litium Battery

The lift of the litium battery is about 1 year and 5 months in continuous use. The voltage between terminals should be higher than 5.1V.

2.2.1.5 Bus Interface Between 16 Bit and 8 Bit System (Figure 2-14)

The GAMYOS board employs the bus interface circuit between the 16 bit and the 8 bit systems. Figure 2-14 diagrams the bus interface circuit.

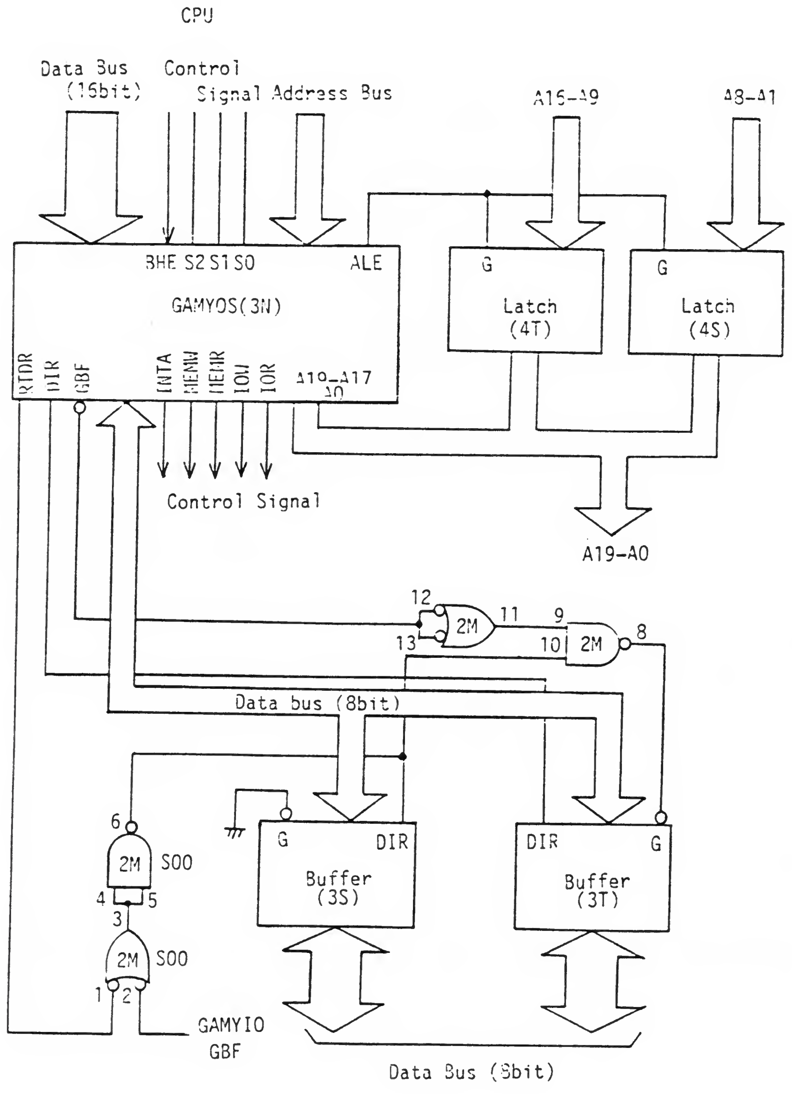


FIGURE 2-14. BUS INTERFACE CIRCUIT

The data conversion 16 bit to/from 8 bit is executed by decoding the BHE signal and $\overline{A0}$ signal.

WRITE CYCLE

Byte transmission

$$\begin{tikzcd}
\overline{A0} = 0 \arrow[r, dash, dashed] & \text{AD7 - AD0} \arrow[dr] & \\
\overline{A0} = 0 \arrow[r, dash, dashed] & \text{AD15 - AD8} \arrow[r] & \text{DA7 - DA0}
\end{tikzcd}$$

Word transmission

$$\begin{tikzcd}
\text{AD7 - AD0} \arrow[r] & \text{DA7 - DA0} \\
\text{AD15 - AD8} \arrow[ur] &
\end{tikzcd}$$

READ CYCLE

Byte transmission

$\overline{A0} = 0$

$\overline{A0} = 1$

$$\begin{tikzcd}
& \text{AD7 - AD0} \\
\text{DA7 -DA0} \arrow[ur] \arrow[r] & \text{AD15 - AD8}
\end{tikzcd}$$

Word transmission

$$\begin{tikzcd}
\text{DA7-DA0} \arrow[r] \arrow[dr] & \text{AD7-AD0} \\
& \text{AD15-AD8}
\end{tikzcd}$$

2.2.2 Memory Control Circuit

Table below shows the memory map on the MCY main control board and Figure 2-15 diagrams the memory control circuit.

MEMORY MAP

00000H	----------------------
	RAM (512 KB)
80000H	----------------------
	RAM (128 KB)
A0000H	----------------------
	reserved for video
B0000H	----------------------
	video RAM
C0000H	----------------------
	I/O expansion
E0000H	----------------------
	I/O expansion
F0000H	----------------------
FC000H	----------------------
	ROM BIOS
FFFFFH	----------------------

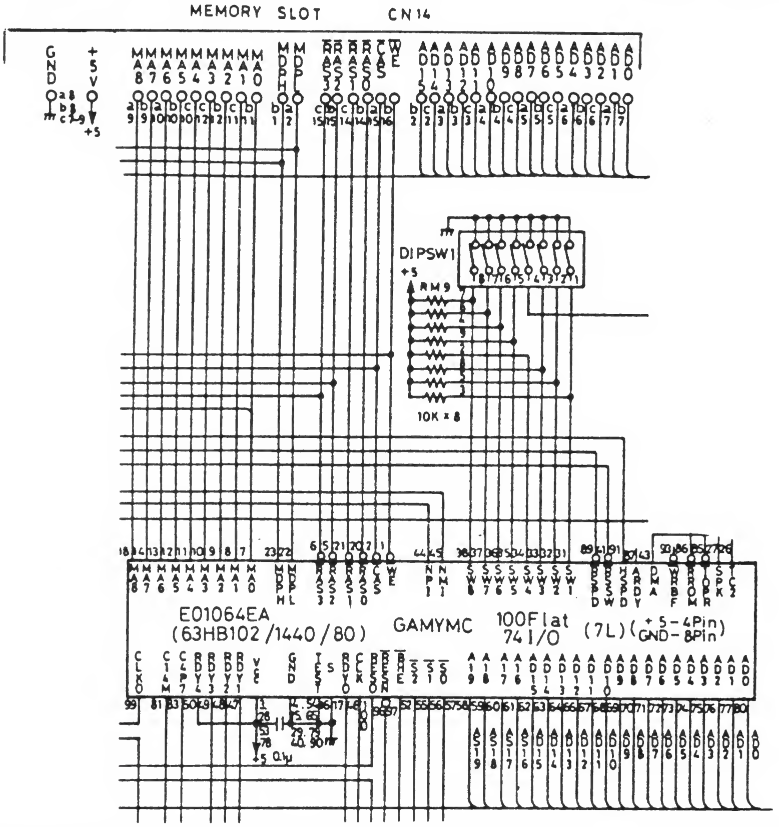
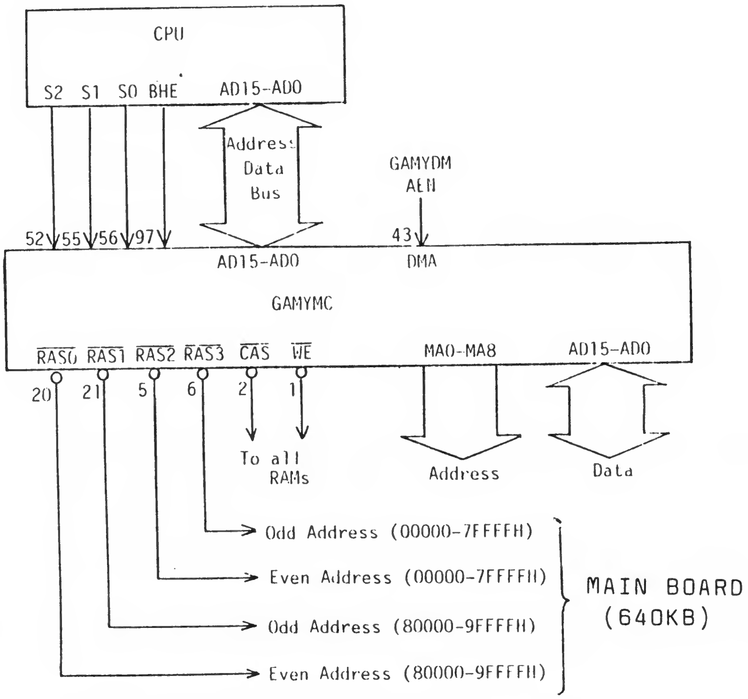


FIGURE 2-15. MEMORY CONTROL CIRCUIT

2.2.2.1 Main Memory Control (Figures 2-16 and 2-17)

The main memory control circuit is diagrammed in Figure 2-16. The GAMYMC provides the main memory control and generates the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and MA0-MA8 signals from the address, $\overline{BHE}$, S0-S2 and DMA signals of the CPU.



B

FIGURE 2-16. MAIN MEMORY CONTROL CIRCUIT

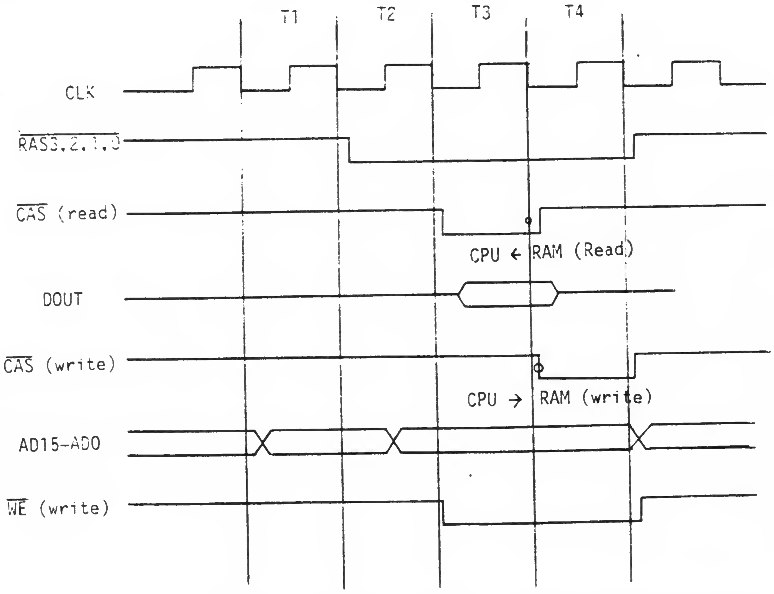


FIGURE 2-17. TIMING DIAGRAM FOR MEMORY ACCESS

2.2.2.2 DRAM Refresh Circuit (Figures 2-18 and 2-19)

The DRAM refresh circuit is also provided by the GAMYMC. The DRAM refresh is executed by using "$\overline{\text{RAS}}$ only refresh mode" of the DRAM.

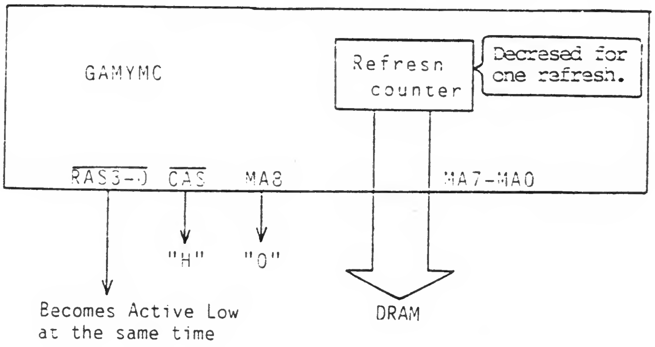

GAMYMC
Refresh counter
Decresed for one refresh.
$\overline{\text{RAS3-0}}$
$\overline{\text{CAS}}$
MA8
MA7-MA0
"H"
"0"
Becomes Active Low at the same time
DRAM

FIGURE 2-18. DRAM REFRESH CIRCUIT

The refresh operation in 4.77MHz clock mode is explained below. The value contained in ( ) is in 7.16MHz clock mode.

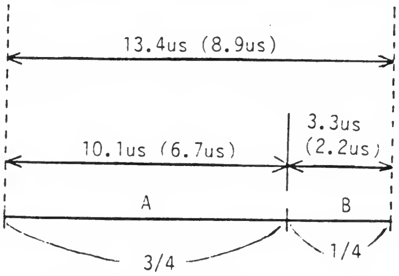


FIGURE 2-19. DRAM REFRESH TIMING

One refresh is executed within each 13.4us period.

Period A : The GAMYMC searches the period which the CPU or the DMAC is not operating DRAM. When detecting in this period, the GAMYMC implements the refresh mode.

Period B : When the GAMYMC cannot execute the refresh operation, that is when period A is used only for DRAM access, the GAMYMC executes the DRAM refresh automatically. If the CPU or the DMAC operates DRAM during the refresh mode in period B, the GAMYMC outputs the READY signal.

In order to refresh the DRAM, three clocks are required.

2.2.2.3 DRAM Parity Check Control Circuit (Figures 2-20 and 2-21)

The GAMYMC generates and checks the parity bit of the DRAM. Figure 2-20 shows the parity bit map for each address and Figure 2-21 diagrams the parity bit output of the GAMYMC.

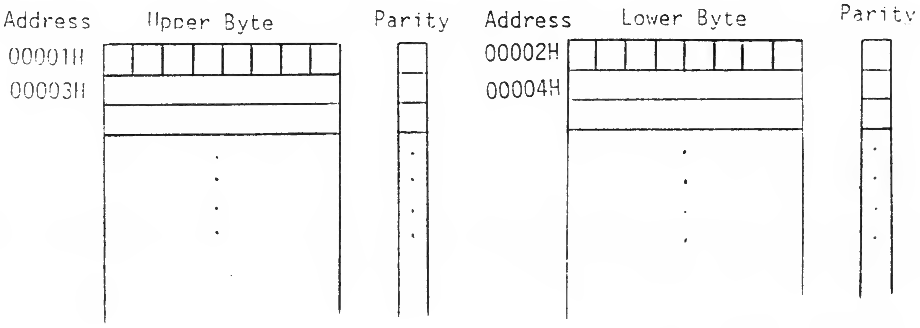


FIGURE 2-20. PARITY BIT MAP

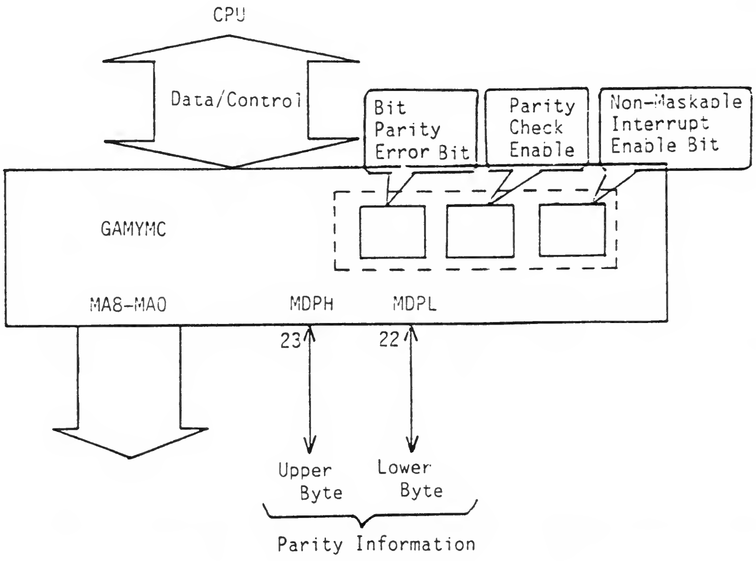


FIGURE 2-21. PARITY BIT OUTPUT OF GAMYMC

Generation of the parity

In DRAM write mode, the GAMYMC calculates the parity and writes the parity bit with data bit.

Parity check

In DRAM read mode, the GAMYMC checks the parity bit. When the parity error occurs, the GAMYMC sets the parity error bit and checks the parity check enable bit and the nonmaskable interrupt enable bit, and if both bit are enable, the GAMYMC outputs the $\overline{\text{NMI}}$ signal.

BIOS ROM Read Circuit

The CPU address F0000H-FFFFFH (64KB) is assigned as the BIOS ROM area. In this are the following ROM combinations can be used.

16 KB (2764 x 2)
32 KB (27128 x 2)
64 KB (27256 x 2)

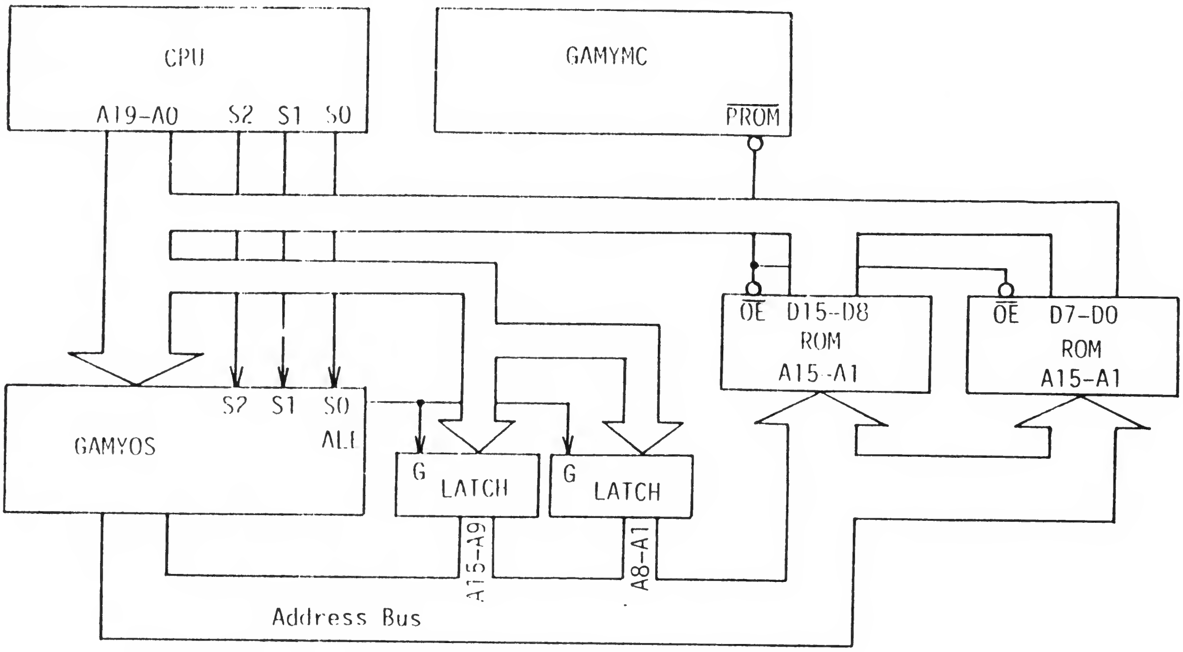


FIGURE 2-22. BIOS ROM READ CIRCUIT

2.2.3 CRT CONTROL CIRCUIT

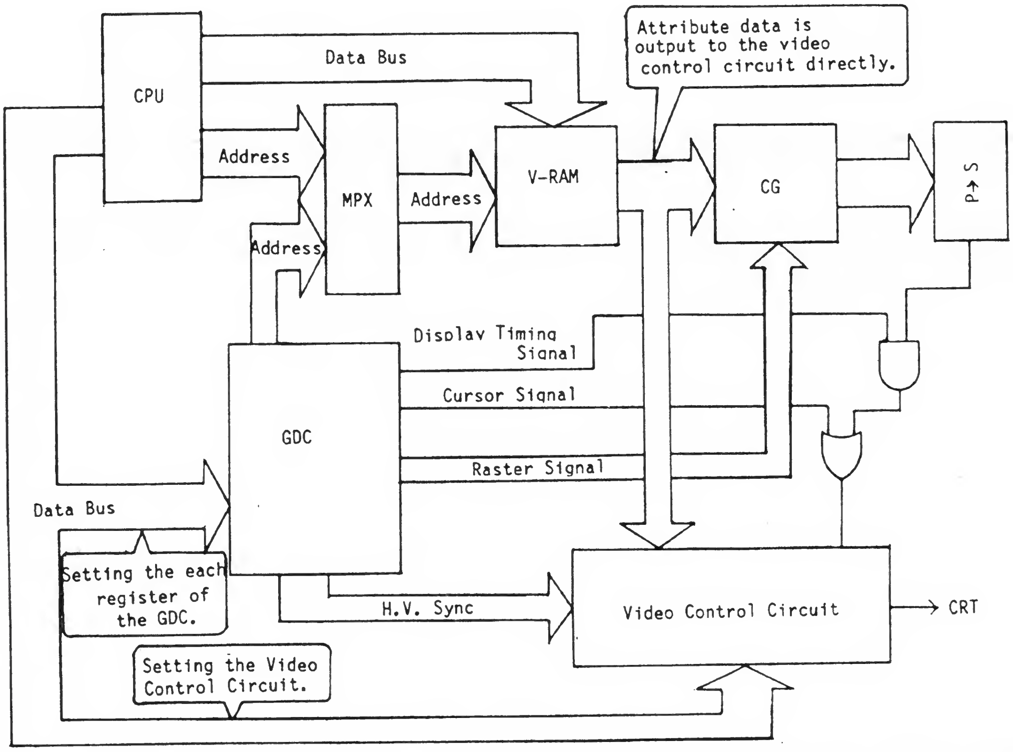
The CRT control circuit features built-in multi-function capabilities, including monochrome text and graphics, and a color text and graphics. The MB89332 in the control circuit is used for graphics display control and also pcrmits vertical scrolling with each dot.

Other features enabled with use of the CRT control circuit are;
64K bytes VRAM (32K words)
Monochrome display with the color monitor (A/N mode)
Reuerse display (monochrome mode)

Whether the CRT control circuit operates in monochrome or color graphics mode depends on the software setting of the configuration register. B
After the configuration register is set the selection of the character generator (CG) and the polarity of H.sync and V.sync is changed automatically by software.

2.2.3.1 **SIGNAL FLOW** (Figures 2-23 through 2-29)

The CRT control circuit has two modes - character display mode and graphic display made.
Figure 2-23 shows the signal flow for the charactor display mode.



Attribute data is output to the video control circuit directly.

Setting the each register of the GDC.

Setting the Video Control Circuit.

FIGURE 2-23. CHARACTER DISPLAY MODE

Figure 2-24 shows the graphic display mode.

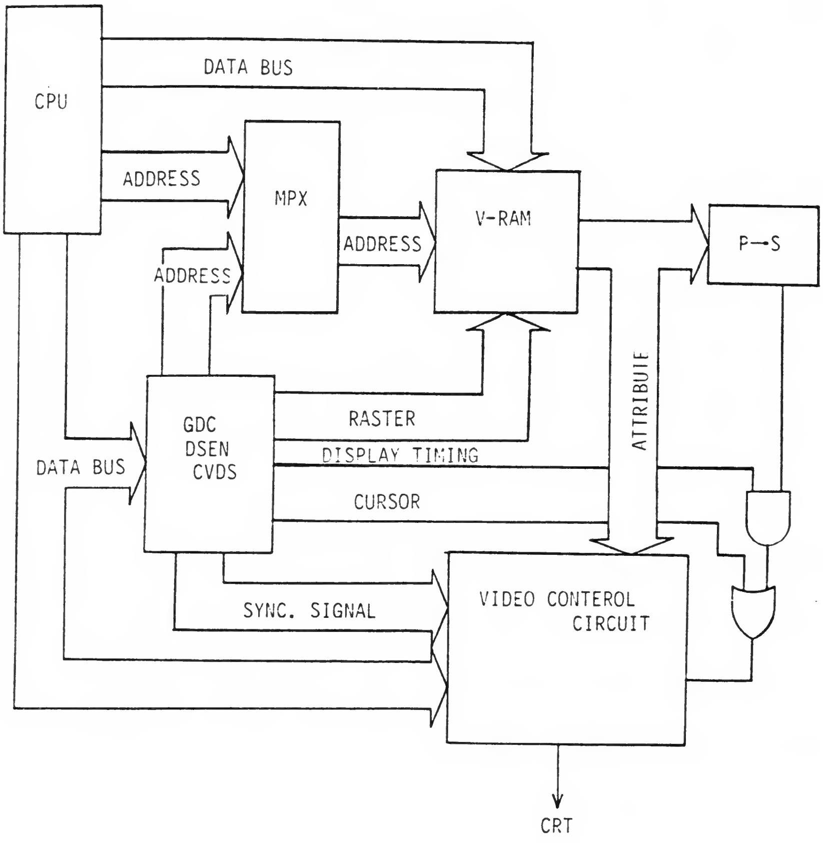


FIGURE 2-24. GRAPHIC DISPLAY MODE

The signal flow for the monochrome and the color display modes are the same as the graphics display mode.

CPU TO GDC

The CPU interface circuit of the CRT control circuit is diagrammed in Figure 2-25.

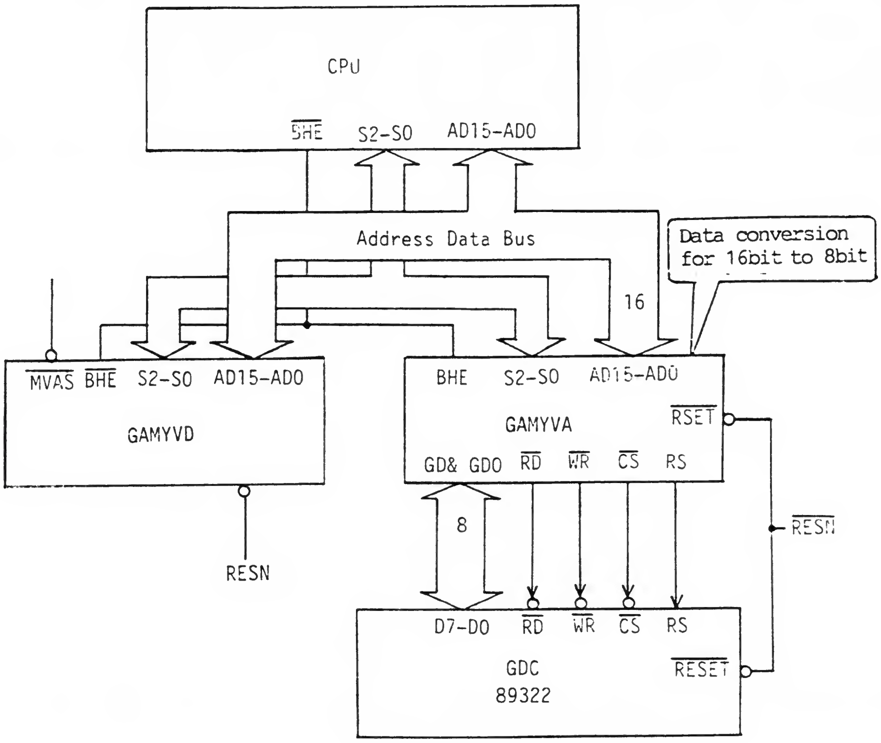


FIGURE 2-25. CPU INTERFACE CIRCUIT OF THE CRT CONTROL CIRCUIT

The principles of operation of the CRT control circuit are described below. The CPU access to the gate array internal register is excuted with CPU signals AD15-AD0, S2-S0 and BHE. The gate array GAMYVA decodes the address data and the status information from the CPU and supplies CS, RS RD and WR signals. The GAMYVA converts the 16 bit data to the 8 bit data. In the CPU write mode to the GDC, it is possible to write with both mode of the byte data unit and the word data unit.
However, in the CPU read mode from the GDC internal register, the byte data unit mode only can be executed. Figures 2-26 through 2-29 show the timing diagrams in the CPU access mode the GDC. The wait cycle is inserted in the write mode with the word only in the data unit.

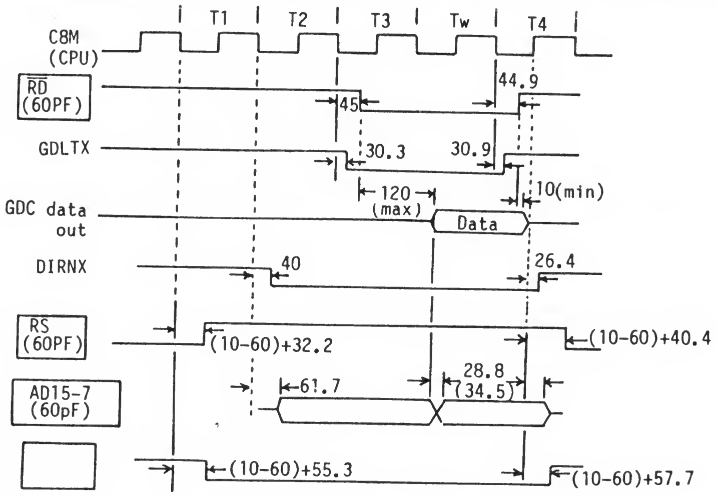


FIGURE 2-26. CPU READ MODE FROM GDC

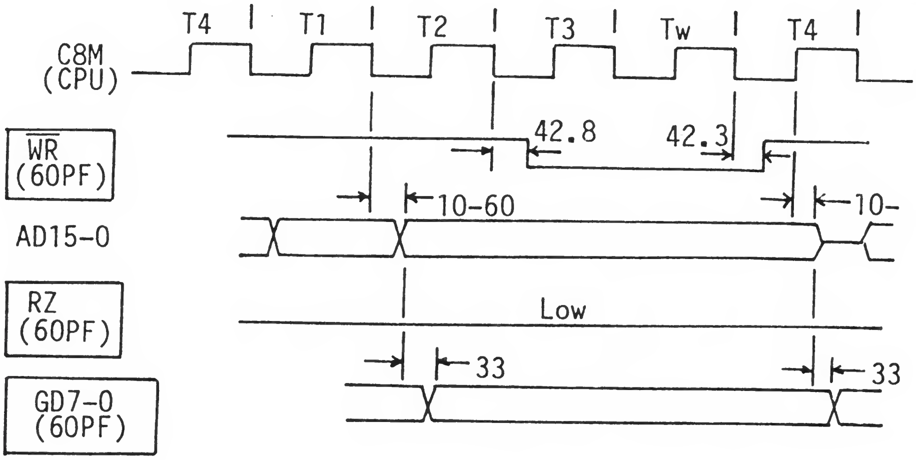


FIGURE 2-27. CPU WRITE MODE TO GDC
(Byte : even)

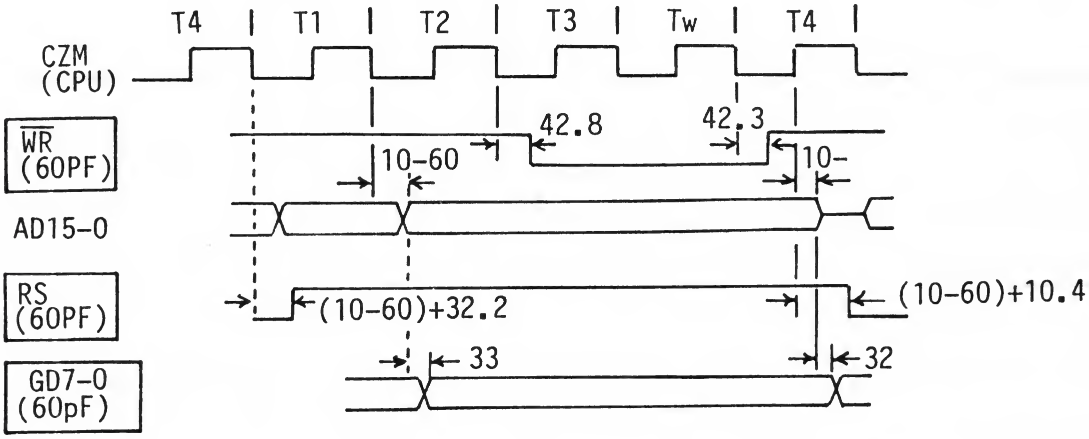


FIGURE 2-28. CPU WRITE MODE TO GDC (Byte : odd)

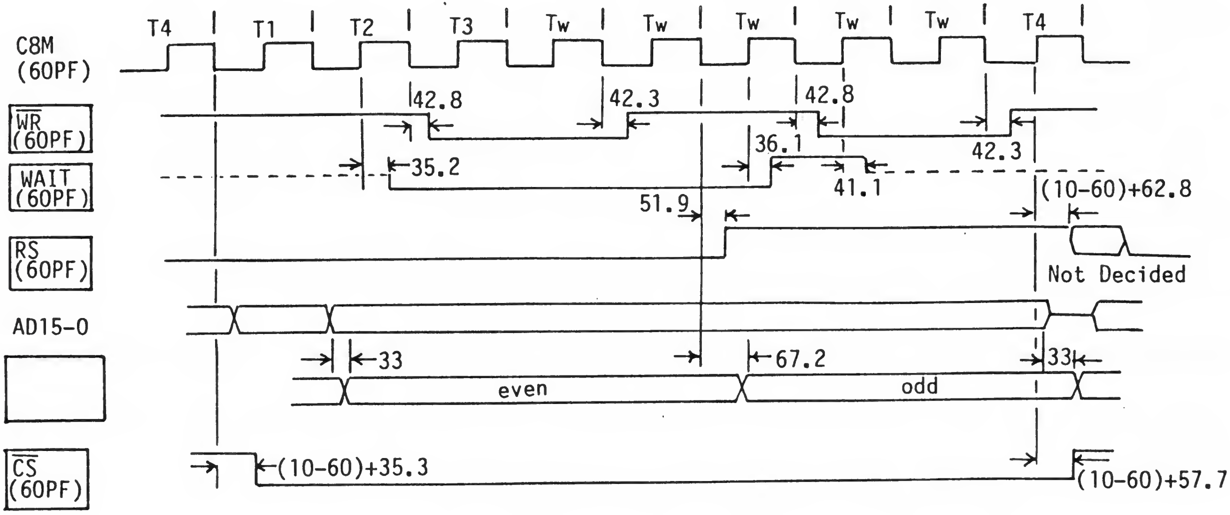


FIGURE 2-29. CPU WRITE MODE TO GDC (Word)

2.2.3.2 I/O REGISTER ADDRESS MAP FOR THE CRT CONTROL CIRCUIT

Table 2-2 shows the I/O register address map for the CRT control circuit. The register 11B0H and 11B1H can be selected at any time by selecting it's I/O port address (11B0H). The registers except 11B0H and 11B1H can be selected at initial reset.

TABLE 2-2. I/O REGISTER ADDRESS MAP

	READ							
	bit7	6	5	4	3	2	1	0
3B4 3D4								
3B5 3D5	MB89322 (Data Register)							
3B8								
3BA	Display status port							
	VSYNC				VIDEO			HSYNC
3BF								
3D8								
3D9								
3DA	Display Status REG.							
					VSYNC	1 $\overline{\text{LPSW}}$	0 LPEW	$\overline{\text{DISP}}$
11B0								
11B1	FONT SEL.REG							
								5X7/7X7

	WRITE							
	bit7	6	5	4	3	2	1	0
3B4 3D4	MB89322 (Index Register)							
3B5 3D5	MB89322 (Data Register)							
3B8	Mode-control Port							
	P1/P0		BLEN		VEN		$\overline{\text{TX}}$/GR	
3BA								
3BF	Herc.Config. SW							
							$\overline{\text{Mask}}$ P1	Prev GR
3D8	Mode control REG.							
			BLEN	HGR	VEN	B/W	GR	HCH
3D9	Color REG.							
			CSEL	BACKI	I	R	G	B
3DA								
11B0	Video config. REG							
	Color/MON	EXT/CMB	MONO	RVS	VB	VA	64/32	INH
11B1								

The access to the registers 3B0H through 3BFH can be executed only as shown as below.

INH (11B0H , bit 0) ----------- "0"
Color/Mono (11B0H , bit 7) ---- "0"

The access to the registers 3D0H through 3DH can be executed only as shown as below.

INH (11B0H , bit 0) ----------- "0"
Color/Mono (11B0H , bit 7) ---- "1"

2.2.3.3. CPU TO VRAM (Figure 2-30)

Figure 2-30 shows the signal flow for CPU access to the VRAM. The VRAM is allocated a part of the CPU memory area, B8000H through BFFFFH.

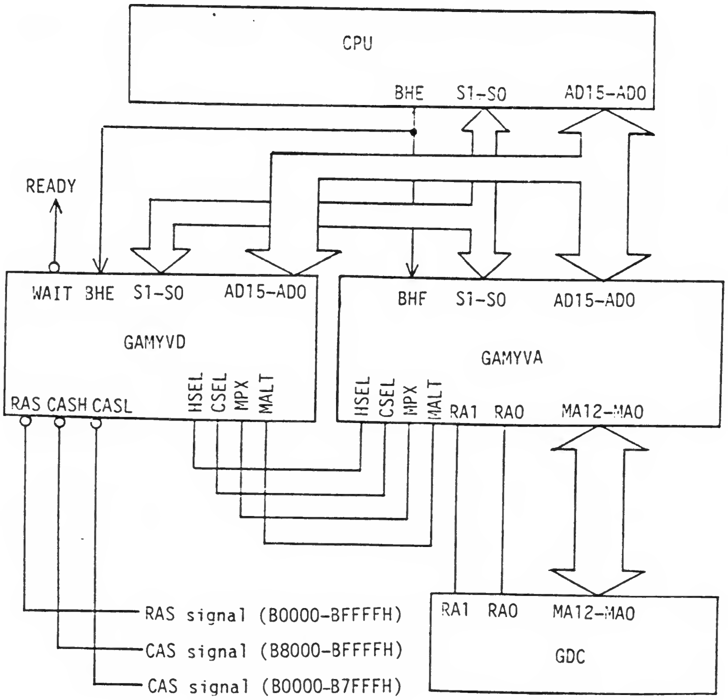


FIGURE 2-30. SIGNAL FLOW FOR CPU TO VRAM

Table 2-3 shows the CPU status signal combinations in each mode of VRAM access.

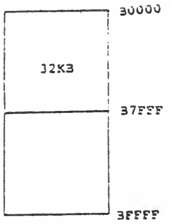
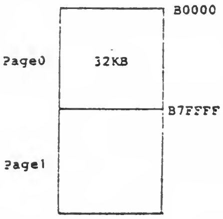
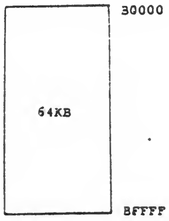
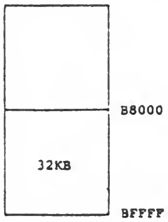
TABLE 2-3. CPU STATUS SIGNAL CONBINATIONS FOR VRAM ACCESS MODE

	BHE	AO	VPPER BYTE WEH1, WEL1	LOWER BYTE WEHO,WELO
WORD ACCESS	0	0	ACTIVE	ACTIVE
WORD ACCESS(*)	0	1	ACTIVE	INACTIVE
	1	0	INACTIVE	ACTIVE
BYTE ACCESS	1	0	INACTIVE	ACTIVE
BYTE ACCESS	0	1	ACTIVE	INACTIVE

(*) Twice memory access is required.

The GAMYVD outputs CSEL and MPX signals and the GAMYVA outputs VRAM address signals. The GAMYVD outputs/inputs video data to/from the VRAM with RAS, CAS and WE signals.
The GAMYVD outputs the address (8 bits) and the column address (6 bits) for the VRAM. Each address signal is latched with the RAS and the CAS signal which are output from the GAMYVD. The CPU access to VRAM is controlled by the setting of the configuration register (11B0H).
Table 2-4 shows the condition for the CPU access to VRAM.

TABLE 2-4. CONDITION FOR CPU ACCESS TO VRAM

11B0H			3B8H		CPU ACCESSABLE AREA (MEMORY ADDRESS MAP)
BIT 0 INH	BIT 6 EXT/CMP	BIT 7 COLOR/MONO	BIT 1 TX/GR	BIT 1 MASK P1	
1	-	-	-	-	Impossible to access VRAM by CPU (External device can use)
0	1	-	-	-	Possible to access the 64KB area - B0000 -BBFFFFH by CPU
	0	0	0	-	 TX MODE(Monochrome) Possible to use the remain area by the external devices
			1	0	 GR MODE (MONOCHROME) Page 1 is masked. Possible to use the remain area by the external devices.
				1	 GR MODE (MONOCHROME) Page 1 is not masked. (Color)
		1	-	-	 A/N and APA mode Possible to use the remain area by the external devices.

Note : The CPU access enable area is different from the GDC VRAM access area.

2.2.3.4 GDC ACCESS TO VRAM (Figures 3-31 through 3-39)

The GDC access to VRAM is executed when the CPU status signal and RA0 through RA1 are supplied; the GDC then supplies row address data for the selected video display character.

The CRT control circuit has the following four modes.

(1) TX mode (monochrome) ------ 80 x 25 (Character mode)

(2) GR mode (monochrome) ------ 720 x 348 (Graphic mode)

(3) A/N mode (color) ---------- 80 x 25 or 40 x 25 (Character mode)

(4) APA mode (color) ---------- 640 x 200 or 320 x 200 dots (Graphic mode)

Figures 2-31 through 2-34 show the VRAM configuration map for each display mode.

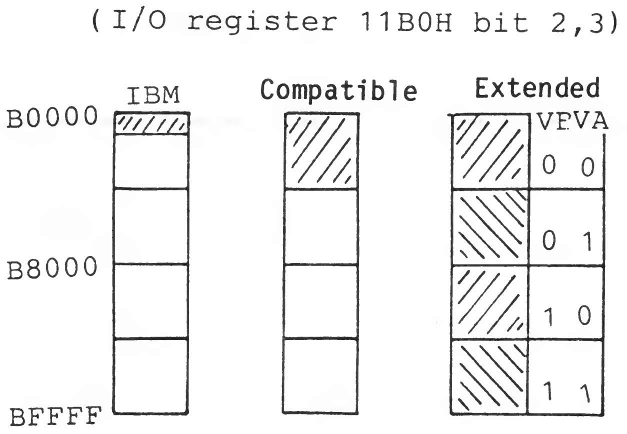


FIGURE 2-31. VRAM CONFIGURATION IN TX MODE

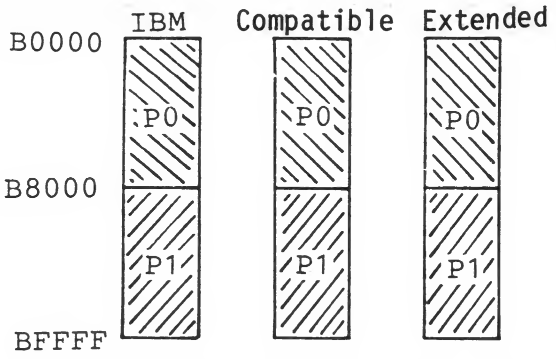


FIGURE 2-32. VRAM CONFIGURATION IN GR MODE

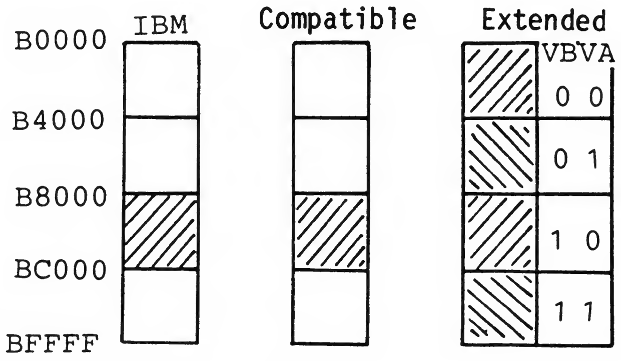


FIGURE 2-33. VRAM CONFIGURATION IN A/N MODE

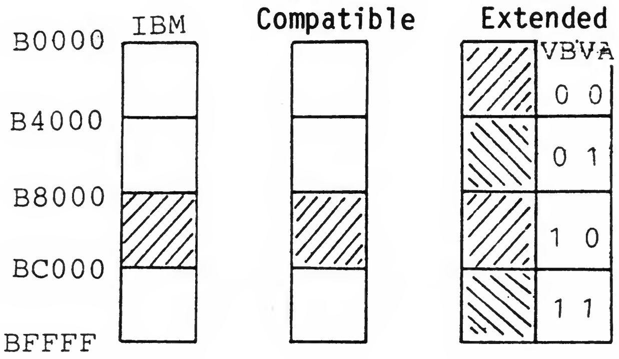


FIGURE 2-34. VRAM CONFIGURATION IN APA MODE

The physical address of VRAM is different from the VRAM address which is allocated as a part of the CPU memory address. The operations of the VRAM access circuit in each display mode are described below. B

VRAM PHYSICAL ADDRESS	
1	0
3	2
5	4
⋮	⋮
FFFD	FFFC
FFFF	FFFE

ADDRESS VIEWED FROM THE CPU	
B0001	B0000
B0003	B0002
B0005	B0004
⋮	⋮
BFFFD	BFFFC
BFFFF	BFFFE

FIGURE 2-35. VRAM PHYSICAL ADDRESS

TX MODE

The address MA12-MA0 of the GDC are output to the VRAM address directly and the 8kb (16KB) VRAM area buffer. Figure 2-36 shows the circuit block diagram in the TX mode.

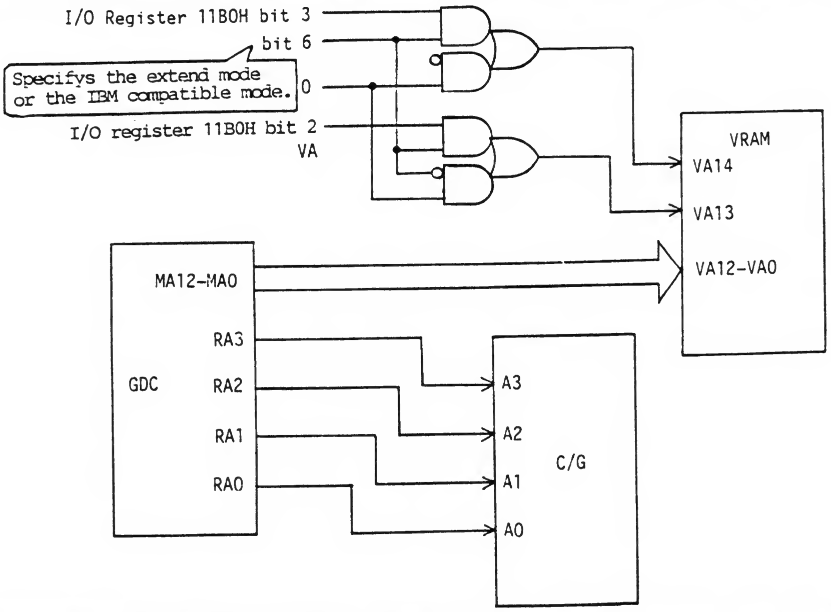


FIGURE 2-36. TX-MODE CIRCUIT BLOCK DIAGRAM

GR MODE

The circuit block diagram is shown in Figure 2-37. In this mode, it is possible to display 348 lines, which are supplied as 4 rasters by 87 display characters. The GR mode uses the VRAM area as 4 divided buffers, each having each 4KW (8KB). One page is composed with the 4 buffers. B

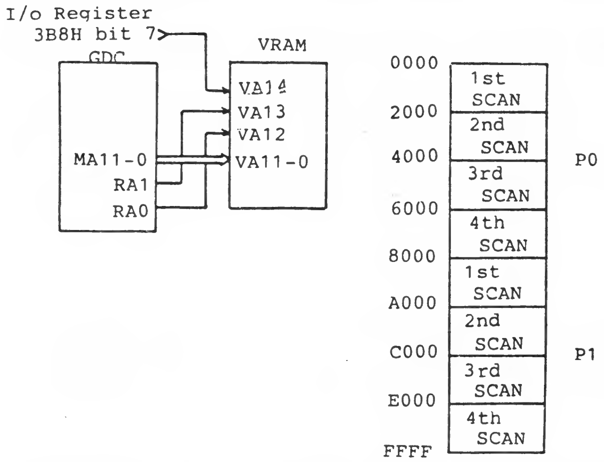


FIGURE 2-37. GR MODE CIRCUIT BLOCK DIAGRAM

A/N MODE

The A/N mode circuit operation is the same as the TX mode, except that the 3-bit raster address, which is supplied by the character generator (CG) is composed with 8 by 8 dots. Figure 2-38 shows the A/N mode circuit block diagram. B

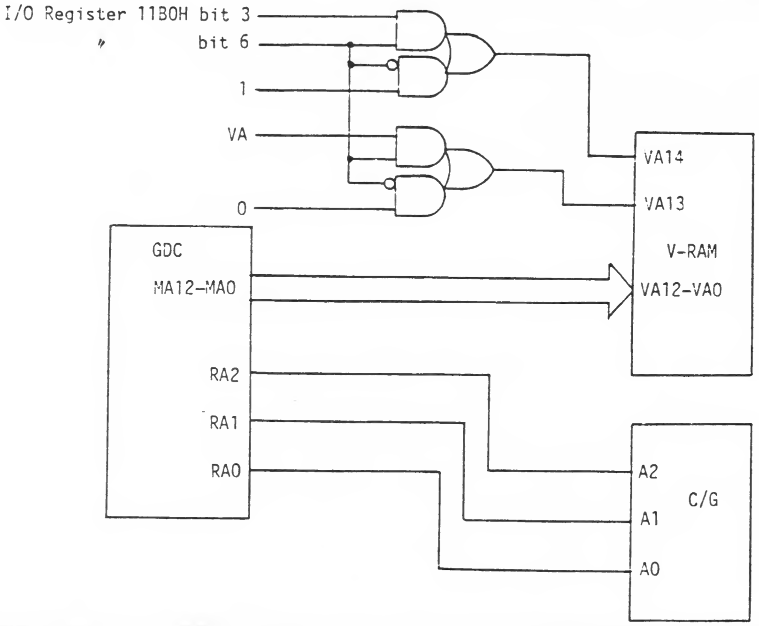


FIGURE 2-38. A/N MODE CIRCUIT BLOCK DIAGRAM

APA MODE

Figure 2-39 shows the APA mode circuit block diagram which is also the same as the TX mode except for the 3-bit raster address. As the A/N mode, the raster address is composed of 8 x 8 dots and is supplied by the character generator. 〈B〉

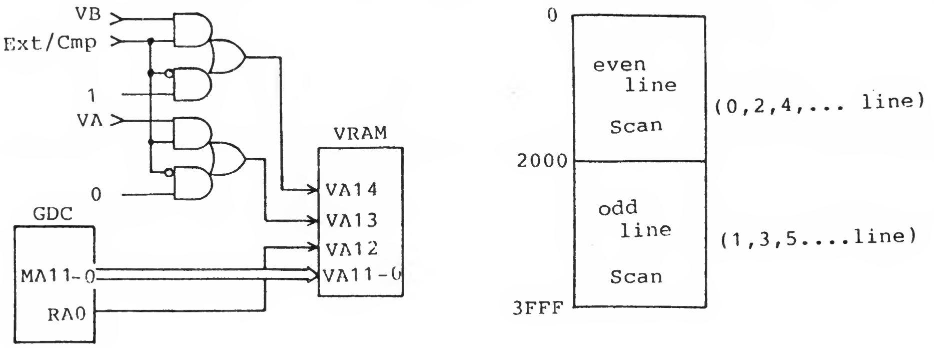


FIGURE 2-39. A/N MODE CIRCUIT BLOCK DIAGRAM

2.2.3.5 VRAM REFRESH

The VRAM refresh is executed by the RAS only refresh mode. The RAS only refresh mode is a refresh mode which refreshes all cells connected to each row address by selecting each 128 row address with only RAS signal during high level CAS signal. The row address signal for VRAM in the VRAM refresh mode is used with the address which is output from the GAMYVD at the time of the VRAM access mode.

2.2.3.6 CHARACTER CLOCK AND DOT CLOCK

The DCLK signal input to the GAMYVD is used for the dot clock, and the CLK signal input to the GDC is used for the character clock. The relationship between the DCLK and CLK signal is shown in Table 2-5.

TABLE 2-5. DCLK SIGNAL AND CLK SIGNAL

MODE	DCLK	CLK
TX mode (9x14)	C16M	C16M/9
GR mode (16x4)	C16M	C16M/16
A/N mode (8x8)	C14M	C14M/8
APA mode (16x2)	C14M	C14M/16

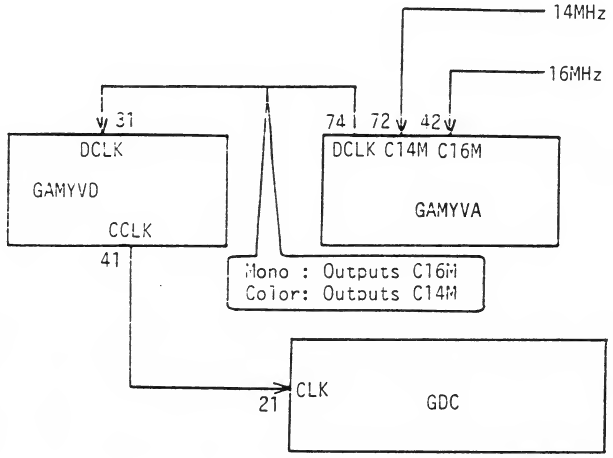
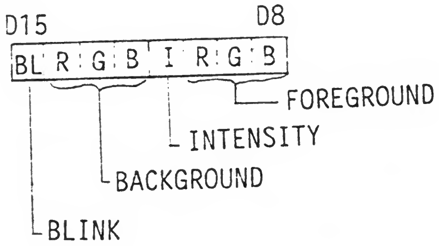
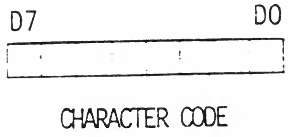


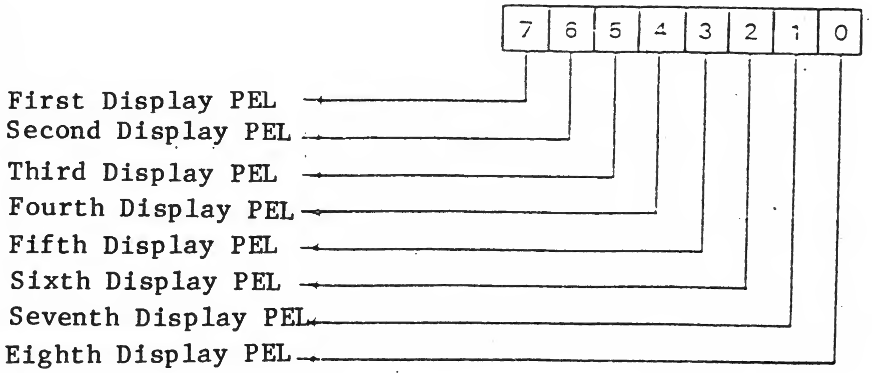
FIGURE 2-40. CHARACTER CLOCK AND DOT CLOCK SUPPLY CIRCUIT

2.2.3.7 **VRAM DATA FORMAT** (Figure 2-40)

Table 2-6 shows the VRAM data format in each display mode.

TABLE 2-6. VRAM DATA FORMAT.

<table>
<tr><th rowspan="2">MODE</th><th colspan="2">DATA FORMAT</th></tr>
<tr><th>UPPER ADDRESS</th><th>LOWER ADDRESS</th></tr>
<tr><td rowspan="2">TX mode
(Monochrome character mode)</td><td> </td><td> </td></tr>
<tr><td colspan="2"><table>
<tr><th colspan="3">Background</th><th colspan="3">Foreground</th><th rowspan="2">Function</th></tr>
<tr><th>R</th><th>G</th><th>B</th><th>R</th><th>G</th><th>B</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Non-Display</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Underline</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>White Character/Black Background</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Reverse Video</td></tr>
</table></td></tr>
<tr><td>A/N mode
(Color character mode)</td><td colspan="2"><table>
<tr><th colspan="8">Attribute Byte</th><th colspan="8">Display-Character Code Byte</th></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
</table>
<table>
<tr><th rowspan="4">Attribute Function</th><th colspan="8">Attribute Byte</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><th>B</th><th>R</th><th>G</th><th>B</th><th>I</th><th>R</th><th>G</th><th>B</th></tr>
<tr><th>FG</th><th colspan="3">Background</th><th colspan="4">Foreground</th></tr>
<tr><td>Normal</td><td>B</td><td>0</td><td>0</td><td>0</td><td>I</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Reverse Video</td><td>B</td><td>1</td><td>1</td><td>1</td><td>I</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Nondisplay (Black)</td><td>B</td><td>0</td><td>0</td><td>0</td><td>I</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Nondisplay (White)</td><td>B</td><td>1</td><td>1</td><td>1</td><td>I</td><td>1</td><td>1</td><td>1</td></tr>
</table>
I = Highlighted Foreground (Character)
B = Blinking Foreground (Character)</td></tr>
</table>

<table>
<tr><th rowspan="2">MODE</th><th colspan="2">DATA FORMAT</th></tr>
<tr><th>UPPER ADDRESS</th><th>CHARACTER CODE</th></tr>
<tr><td>A / N</td><td colspan="2">
<table>
<tr><th>R</th><th>G</th><th>B</th><th>I</th><th>Color</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Blue</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Red</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Brown</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>White</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Gray</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Light Blue</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Light Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Light Cyan</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Light Red</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Light Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>White (High Intensity)</td></tr>
</table>
</td></tr>
<tr><td>GR mode</td><td colspan="2">

7
6
5
4
3
2
1
0
First Display PEL
Second Display PEL
Third Display PEL
Fourth Display PEL
Fifth Display PEL
Sixth Display PEL
Seventh Display PEL
Eighth Display PEL

</td></tr>
</table>

MODE	DATA FORMAT	
	UPPER ADDRESS	LOWER ADDRESS

APA

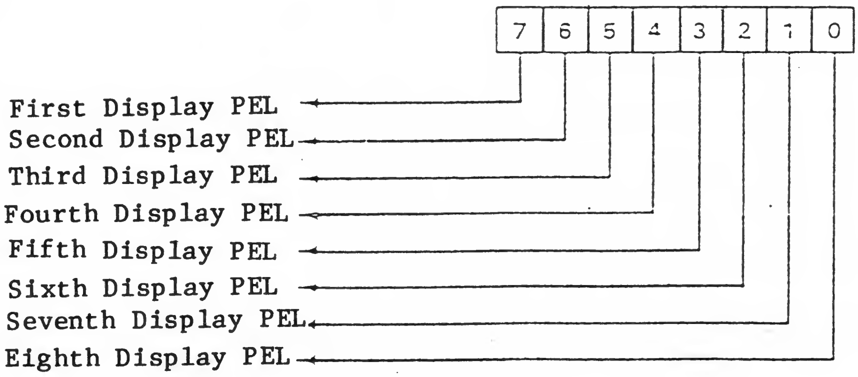
(320 x 200)

D7	D6	D5	D4	D3	D2	D1	D0
C1	C0	C1	C0	C1	C0	C1	C0
First dispaly PEL		2 "		3 "		4 "	

	CSEL	0	0	1	1
C1	C0 BACKI	0	1	0	1
0	0	Specify the background color with I/O register 3D9H bit 0-3			
0	1	GREEN	LIGHT GREEN	CYAN	LIGHT CYAN
1	0	RED	LIGHT RED	MAGENTA	LIGHT MAGENTA
1	1	BROWN	YELLOW	WHITE	WHITE (I)

APA

(640 x 200)



2.2.3.8 Composit Signal Generator Circuit (Figure2-41)

The monitor composite signal is generated by the circuit (shown in Figure 2-41) and synchronous signals. The composite signal is composed of video signals R, B and I.

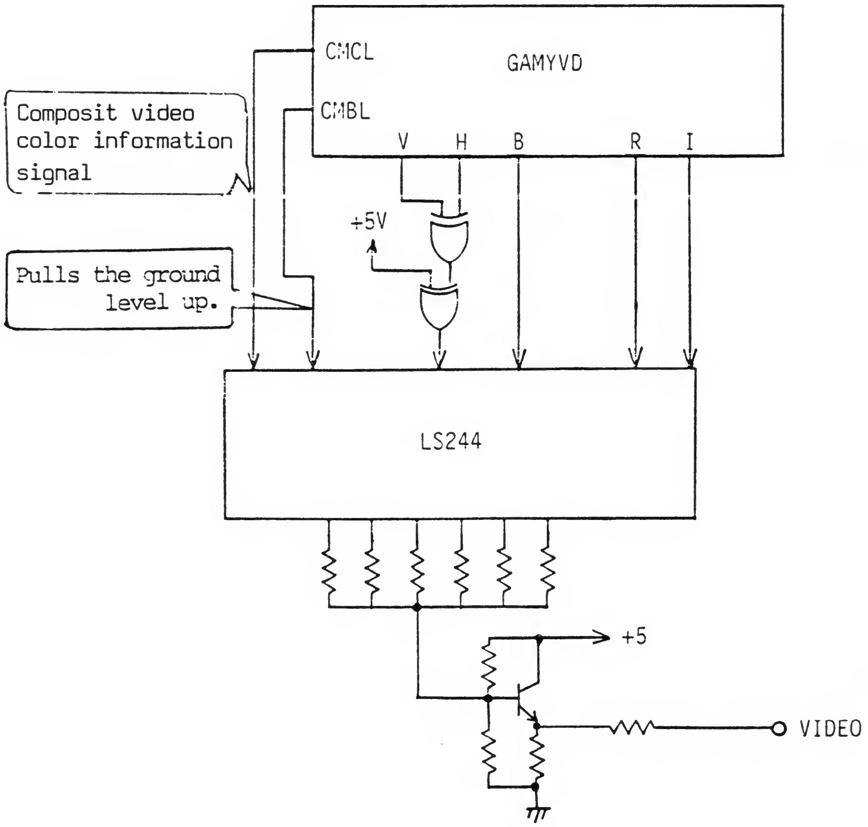

CMCL
CMBL
GAMYVD
V
H
B
R
I
Composit video color information signal
Pulls the ground level up.
+5V
LS244
+5
VIDEO

FIGURE 2-41. COMPOSITE SIGNAL GENERATOR CIRCUIT

2.2.3.9 Character Generator

The 8KB 2764 is used for the character generator. The following three type font sets are stored in the ROM.

9 x 14 dots for the monochrome CRT --------- 1 type (4KB)
8 x 8 dots for the color CRT --------------- 2 type (2KB x 2)

2.2.4 DMA Control Circuit (Figures 2-42 through 2-46)

The DMA control circuit block diagram is shown in Figure 2-42.

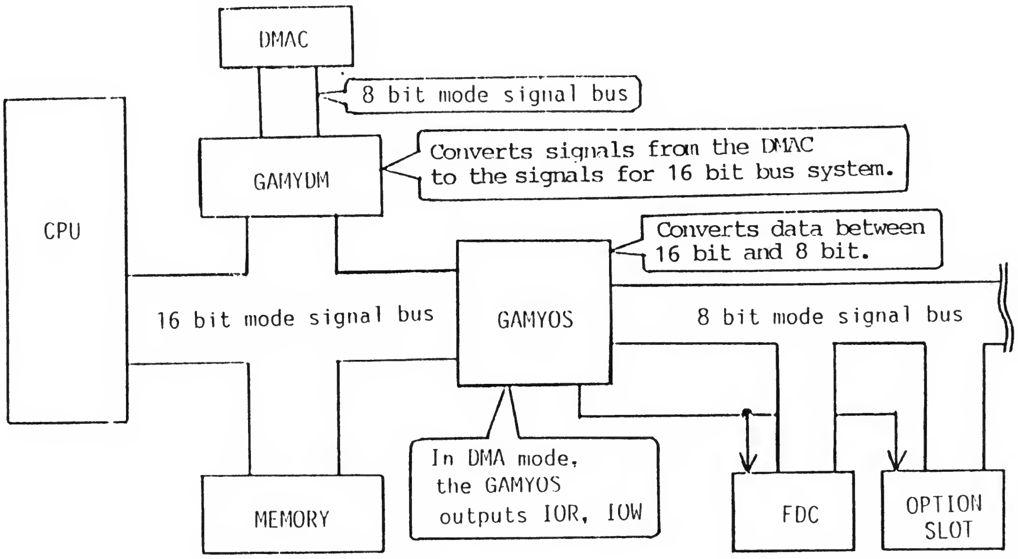

DMAC
8 bit mode signal bus
CPU
GAMYDM
Converts signals from the DMAC to the signals for 16 bit bus system.
Converts data between 16 bit and 8 bit.
16 bit mode signal bus
GAMYOS
8 bit mode signal bus
In DMA mode, the GAMYOS outputs IOR, IOW
MEMORY
FDC
OPTION SLOT

FIGURE 2-42. DMA CONTROL CIRCUIT BLOCK DIAGRAM

The DMA control circuit supports two DMA modes, memory to I/O and I/O to memory. All I/O devices which request the DMA transfer are connected to the 8-bit data bus.

The DMA control circuit is provided with the 8237 DMA controller and two gate arrays, GAMYDM and GAMYOS. The operation of the DMA control circuit is discussed in the sections following and includes discussion of: ⟨B⟩

(1) Setting of the DMAC and the page register
(2) DMA sequence

(1) Setting of the DMAC and the page register

The following two settings are required to execute the DMA transfer. Figure 2-43 shows the circuit which connects between the DMAC and the CPU

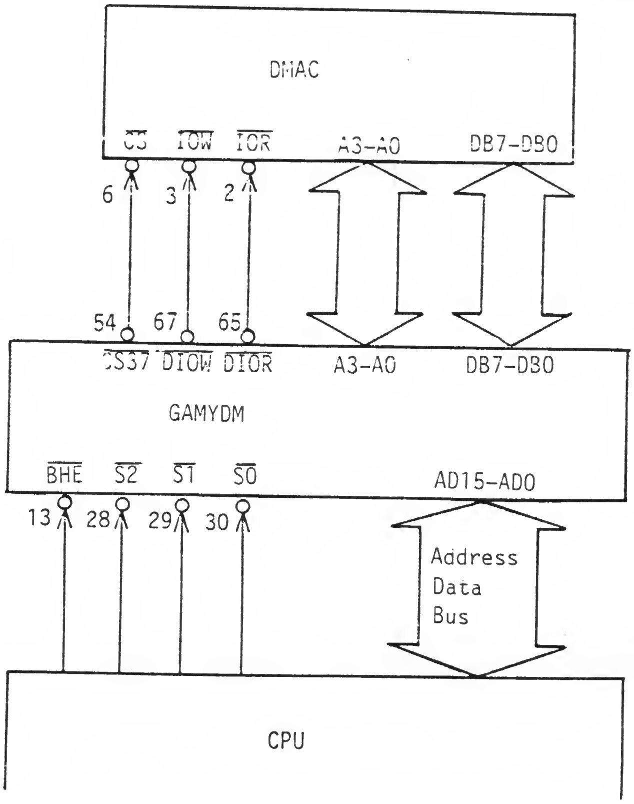


FIGURE 2-43. CONNECTION BETWEEN DMAC AND CPU

The setting sequence is described below:

1. The GAMYDM latches the address output from the CPU with the ALE signal provided by the PS0-PS2 signal from the CPU.

2. The GAMYDM decodes the address information latched and outputs the CS37 signal. The lower 4-bit address of the GAMYDM is connected to the 8237 DMAC.

3. The CPU outputs the address data for the internal address register of the DMAC and the word count data for the internal word count register of the DMAC.

Page Register Setting

The DMA address register of the DMAC is comprised of 16-bit and twenty address lines from the V30 CPU, to provide 1M-byte of memory area. The page register employs the control for the upper 4-bit address; it can also be operated as an I/O port. B

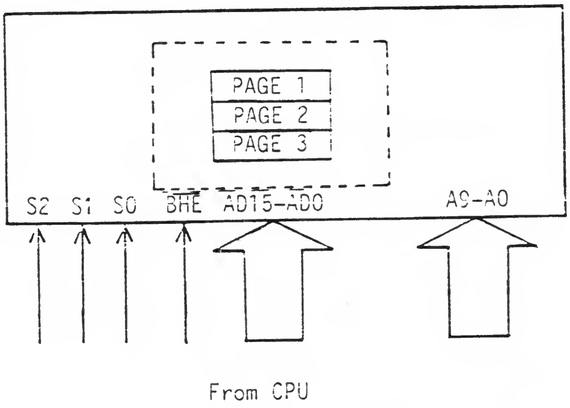


FIGURE 2-44. PAGE REGISTER OF DMAC

(2) DMA sequance

The DMA sequence includes two functions:

a. DMA request and acknowledge from the external devices
b. DMAC control for the I/O devices and the memory B

a. DMA request and acknowledge from the external devices

All DMA request signals on the MCY main control board are connected to the option slot. When using the DRQ2 signal on the option slot, the DRQ2 signal from the FDC must be masked with the controlling DMA signal of the GAMYIO. B

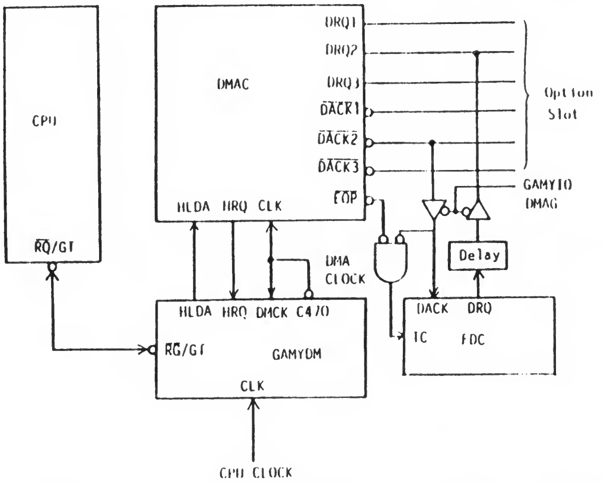


FIGURE 2-45. DMA CONTROL CIRCUIT

b. DMAC control for the I/O devices and the memory

Figure 2-46 shows the signal flow chart of the DMA control circuit.

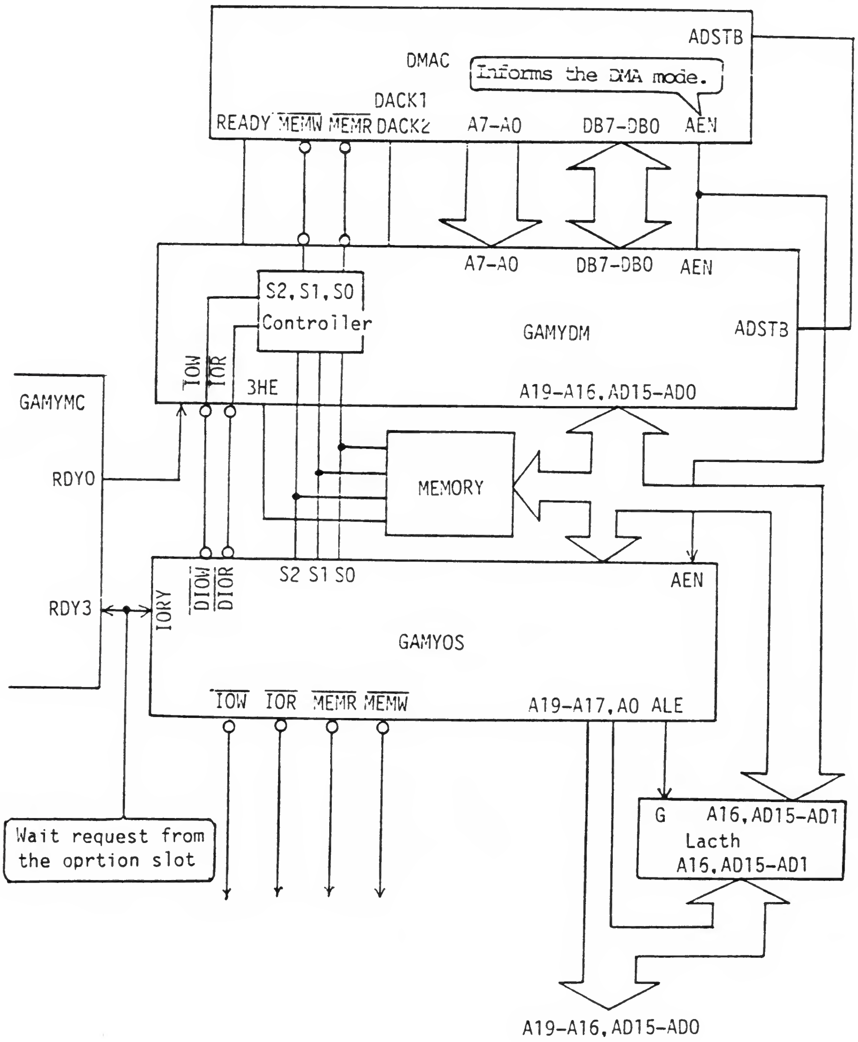


FIGURE 2-46. DMA CONTROL CIRCUIT SIGNAL FLOWCHART

Memory Address

Memory address A19-A16 are output from the page register of the GAMYDM. The upper address lines, A19 through A14, are software controlled. B

$\overline{\text{IOR}}$, $\overline{\text{IOW}}$ signals for the DMA request devices

The $\overline{\text{IOR}}$, $\overline{\text{IOW}}$ signal for the DMA request devices are provided with the $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$ of the 8237.

Data Transmission

In DMA mode, data is always transmitted by byte. The relationship between the AD15-AD0 and the DA7-DA0 of the GAMYOS is shown as follows.

Memory to I/O

A0 0 ------- AD7 - AD0 to DA7 - DA0
1 ------- AD15 - AD8 to DA7 - DA0

I/O to memory

A0 0 ------- DA7 - DA0 to AD7 - AD0
1 ------- DA7 - DA0 to AD15 - AD8

2.2.5 Interrupt Control Circuit (Figures 2-47 and 2-48)

The interrupt control circuit (8259 subset) is activated by the interrupt controller on the GAMYIO as it generates the interrupt request signal.

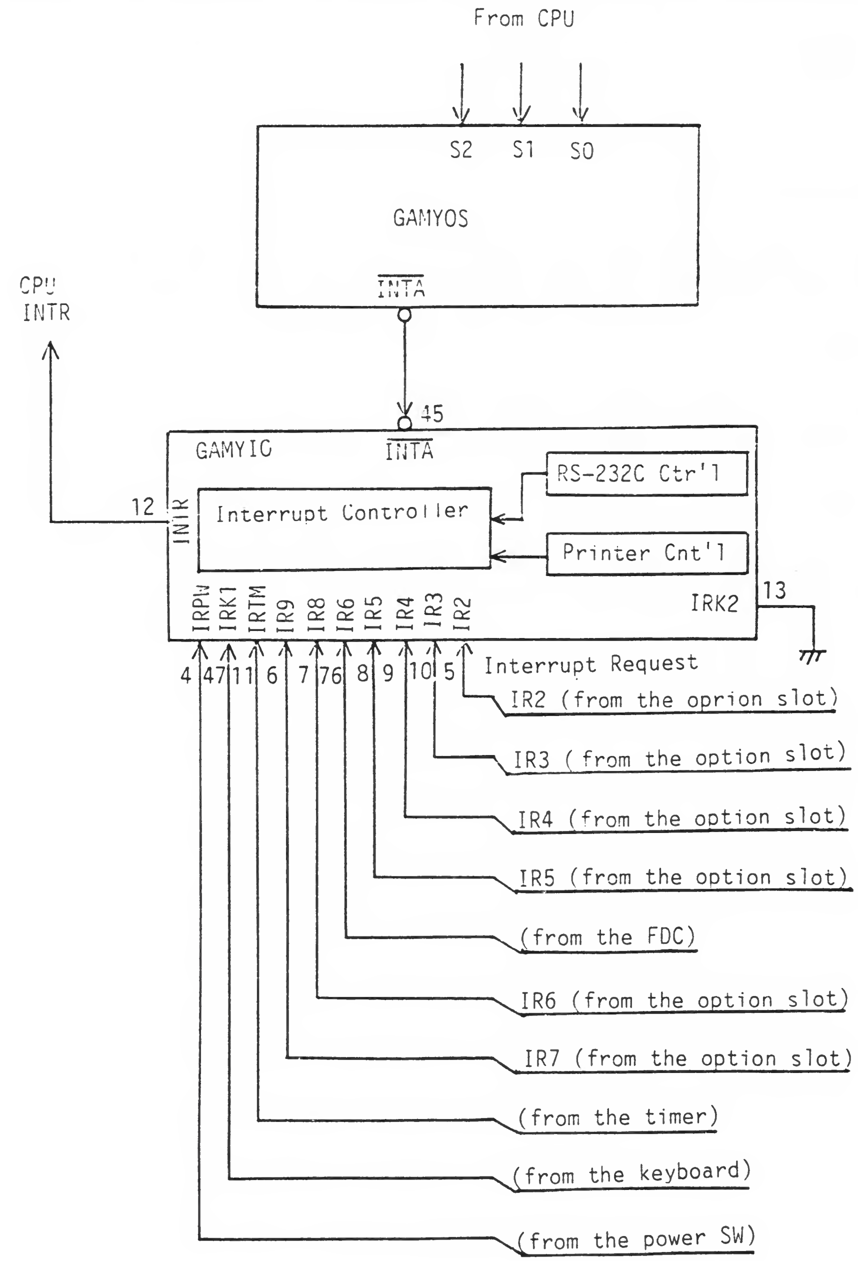


FIGURE 2-47. INTERRUPT CONTROL CIRCUIT

Interrupt Request from the Timer IC

The 8253 timer can request a CPO interrupt.

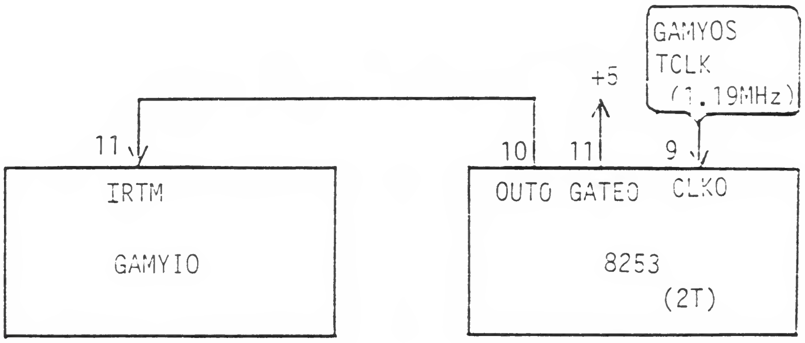


FIGURE 2-48. TIMER INTERRUPT REQUEST

2.2.6 RTC Control Circit (Figures 2-49 and 2-50)

Figure 2-49 diagrams the RTC control circuit. The GAMYOS controls access to the RTC internal register.

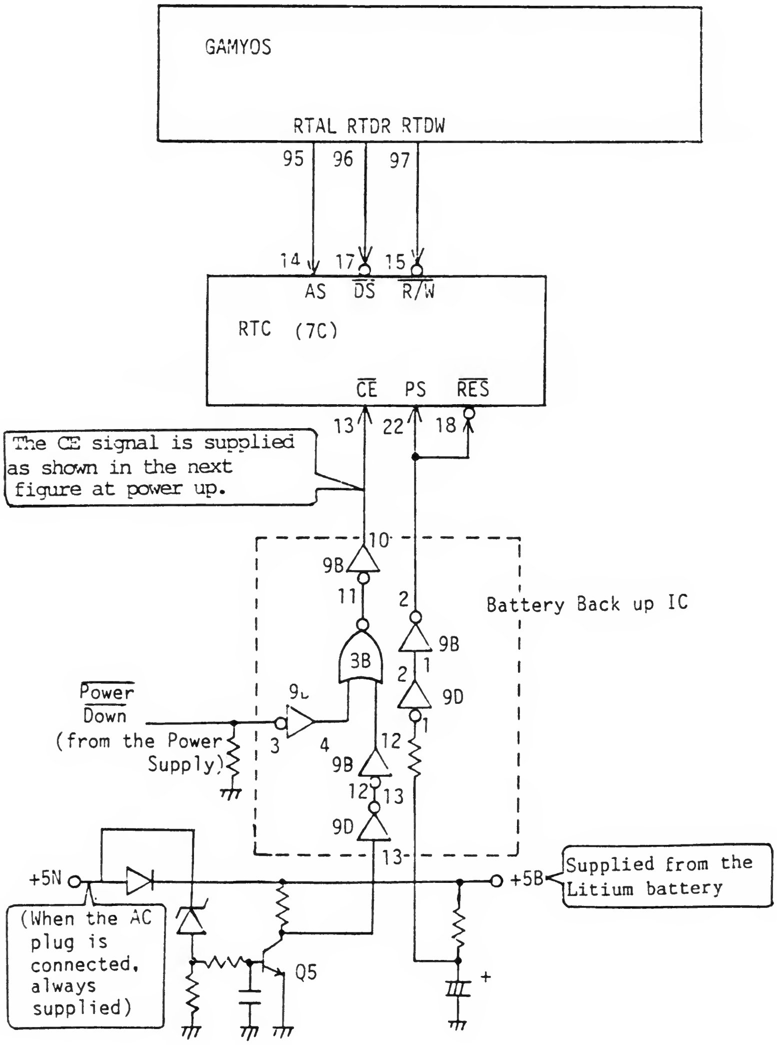

GAMYOS
RTAL RTDR RTDW
95 96 97
14 17 15
AS DS R/W
RTC (7C)
CE PS RES
13 22 18
The CE signal is supplied as shown in the next figure at power up.
10
9B
11
2
Battery Back up IC
3B
9B
1
2
9D
9L
1
Power Down (from the Power Supply)
3
4
12
9B
12
13
9D
13
+5N
+5B
Supplied from the Litium battery
(When the AC plug is connected, always supplied)
Q5
+

FIGURE 2-49. RTC CONTROL CIRCUIT

Access for the RTC Internal Register

In order to read/write to the RTC, two I/O port accesses are required. The first I/O port access for the RTC provides the control register address for the RTC; the second provides data for the RTC. When the CPU reads data from the RTC, the GAMYOS controls the RTDR signal; when the CPU writes data to the RTC, the GAMYOS controls the RTDW signal. The $\overline{\text{CE}}$ signal for the RTC is provided with the power down signal and the +5V voltage detection circuit. Figure 2-50 shows the timing diagram at power ON/OFF. ⟨B⟩

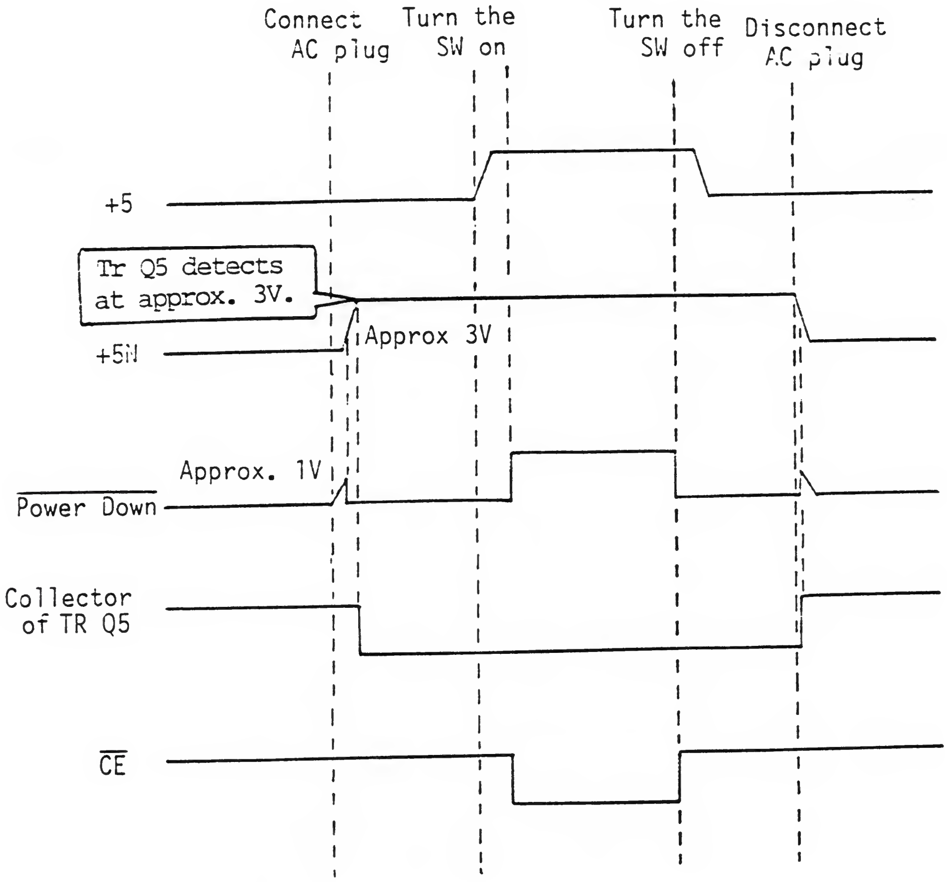


FIGURE 2-50. CE FOR THE RTC TIMING DIAGRAM

When the following conditions are satisfied, the $\overline{\text{RES}}$ and the PS signal become low.

No connection of AC connect.
No power supply from the battery.

2.2.7 **RS-232C CONTROL CIRCUIT** (Figure 2-51 and 2-52)

Figure 2-51 shows the RS-232C control circuit. This circuit is located in the GAMYIO.
The general specifications of the RS-232C control circuit are described below.

Character ------------------ 7 bit or 8 bit
Stop bit ------------------ 1 bit or 2 bit
Parity ------------------ Odd, Even, Non parity or Stick parity.
Data buffer ---------------- Double buffer (transmit / receive mode)
Baud rate ------------------ 50 bps - 56 Kbps
Error detect --------------- Over run, parity error, framing error.
Modem control -------------- $\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, CD.
Interrupt ------------------ Receive complete. Transmit acknowledge, error
Diagnostics ---------------- Loop back, error simulation

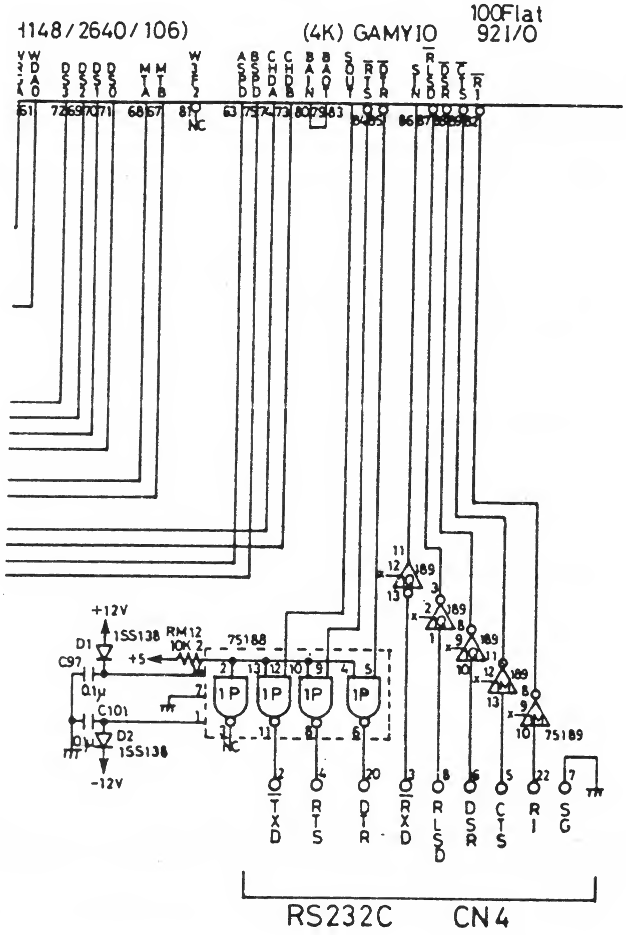


FIGURE 2-51. RS-232C CONTROL CIRCUIT

Figure 2-52 shows the internal block diagram of the GAMYIO.

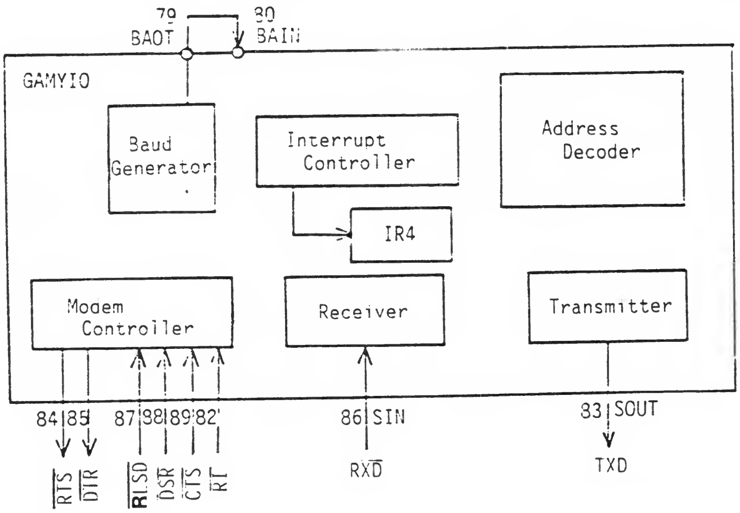


FIGURE 2-52. GAMYIO INTERNAL BLOCK DIAGRAM (RS-232C)

Each control block operates as described below.

Baud rate generator : Generates the baud rate. (Changeable by the settings of the I/O register)

Address decoder : Changes the I/O address and the interrupt levels, e.g. when the option card used has the same address as the GAMYIO. (In case that the option cards which have the same I/O address and interrupt levels are used.) ⟨B⟩

Interrupt controller : Generates the interrupt request signal in the following case.

(1) Error occurs
(2) Data receive is completed
(3) When the transmitter holding register (THR) is vacant
(4) $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RLSD}}$, $\overline{\text{RI}}$ signals are changed.

The interrupt request signal is sent to the interrupt control circuit (8259 subset) which is located in the GAMYIO.

Modem controller : Controls $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ signals and RS-232C interrupt request signal checks $\overline{\text{RI}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ and $\overline{\text{RLSD}}$ signals.

2.2.7.1 **BAUD RATE GENERATOR** (Figure 2-53)

Table 2-7 shows the relationship between the baud rate and the settings of the I/O registers, DLM and DLL.

TABLE 2-7. BAUD RATE SETTINGS

BAUD RATE	VALUE TO BE SET DECIMAL	DLM(HEX)	DLL(HEX)
50	2304	09	00
75	1536	06	00
110	1047	04	17
134.5	857	03	59
150	768	01	00
300	384	00	80
600	192	00	C0
1200	96	00	60
1800	64	00	40
2000	58	00	3A
2400	48	00	30
3600	32	00	20
4800	24	00	18
7200	16	00	10
9600	12	00	0C
19200	6	00	06
38400	3	00	03
56000	2	00	02

The froquency timing diagram of the output from the BAOT terminal of the GAMYIO is shown in Figure 2-53. B

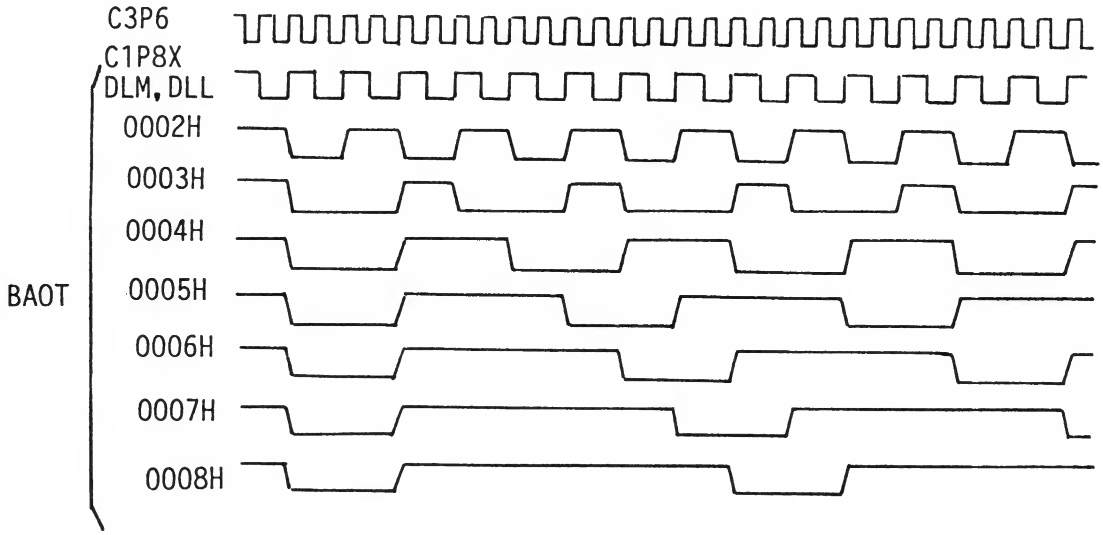


FIGURE 2-53. BAUD DATE GENERATOR TIMING DIAGRAM

2.2.7.2 ADDRESS DECODER

The I/O address for the RS-232C control circuit is supplied by setting bits 7 and 6 of I/O register 11B9H and bit 3 of the modem control register MCR.

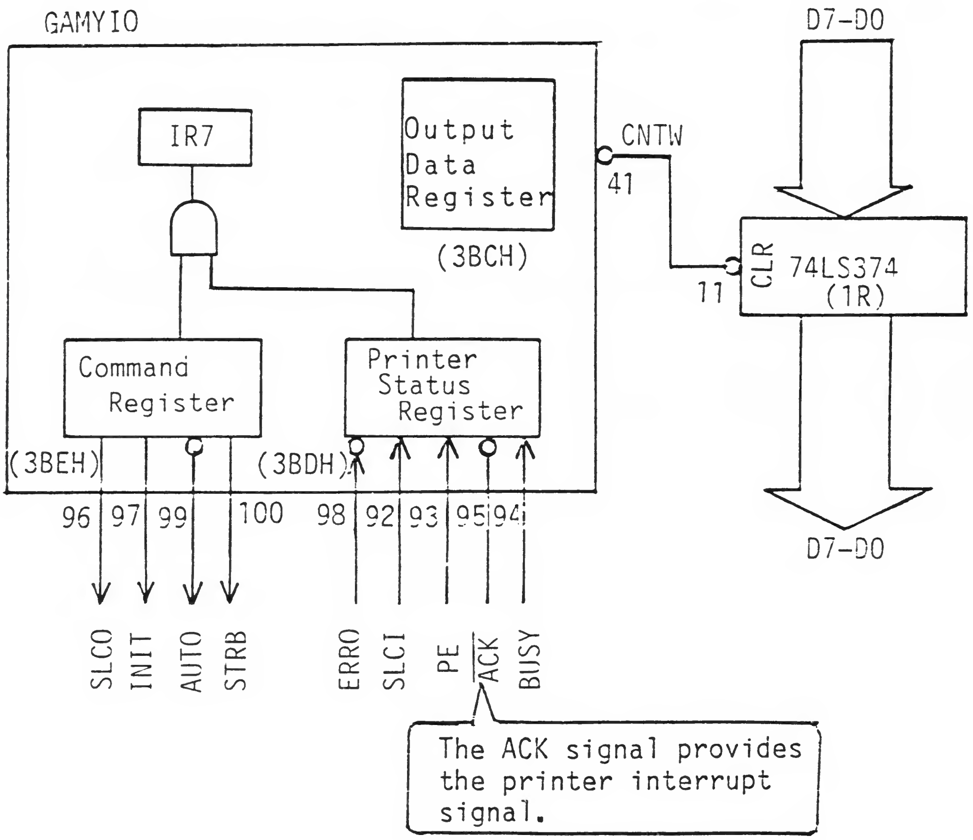
TABLE 2-8. RS-232C CONTROL CIRCUIT ADDRESS DECORER

MCR OUT2	11B9H		RS-232C CIRCUIT (GAMYIO)		OPTION SLOT	
	D7	D6	INTERRUPT	ADDRESS	INTERRUPT	ADDRESS
0	0	0	INVALID	3FxH	IR3 IR4 VALID	2FxH
0	0	1	INVALID	2FxH	IR3 IR4 VALID	3FxH
1	0	0	USES IR4	3FxH	IR3 VALID	2FxH
1	0	1	USES IR3	2FxH	IR4 VALID	3FxH
*	1	*	----	--	IR3 IR4 VALID	2FxH 3FxH

*: Not applicable
MCR OUT2 --- Modem control register bit 3
3FxH ------- 3F8H - 3FEH
2FxH ------- 2F8H - 2FEH

2.2.8 PRINTER INTERFACE CIRCUIT (Figure 2-54)

The printer interface circuit is included in the GAMYIO as shown in Figure 2-54. The output data to 74LS374 (1R) is latched with the CNTW signal.



The ACK signal provides the printer interrupt signal.

FIGURE 2-54. PRINTER INTERFACE CIRCUIT

The output command and printer status registers are the I/O port registers. The address for the three registers are changeable by jumper setting as follows. Table 2-9 shows the JUMP jumper setting.

TABLE 2-9. JUMP SETTINGS

JUMPER SETTING	I/O ADDRESS
INSTALLE	378H-37AH
NOT INSTALLED	3BCH-3BEH

The terminal functions for the printer interface circuit are listed in the following table. ⟨B⟩

TABLE 2-10. PRINTER INTERFACE CIRCUIT TERMINAL FUNCTION

SIGNAL	I/O	FUNCTION
BUSY	I	BUSY SIGNAL
$\overline{\text{ACK}}$	I	ACKNOWLEDGE SIGNAL
PE	I	PAPER EMPTY SIGNAL
SLCI	I	SELECT SIGNAL
$\overline{\text{ERRO}}$	I	ERROR SIGNAL
SLCO	O	SELECT-IN SIGNAL
INIT	O	INITIALIZE SIGNAL
AUTO	O	AUTO-FEED-XT SIGNAL
STRB	O	STROBE SIGNAL
$\overline{\text{CNTW}}$	O	WRITE PULSE FOR THE DATA OUTPUT PORT.

Note: All output signals except $\overline{\text{CNTW}}$ are reversed logically by the external buffer, therefore the output signal from the GAMYIO is reversed logically as viewed from the printer input terminal.

2.2.9 Speaker Control Circuit (Figure 2-55)

Figure 2-55 diagrams the speaker control circuit on the MCY circuit board. The values programmed into counter 2 of 2T are configured as a square wave generator and determine the frequency supplied to the internal speaker. The output signal of counter 2 is supplied to the input terminal of 4D. The other terminal of 4D is an input signal supplied from the GAMYIO. This signal determines the duration of sound generation. When this signal is high, the sound is generated from the internal audio speaker.

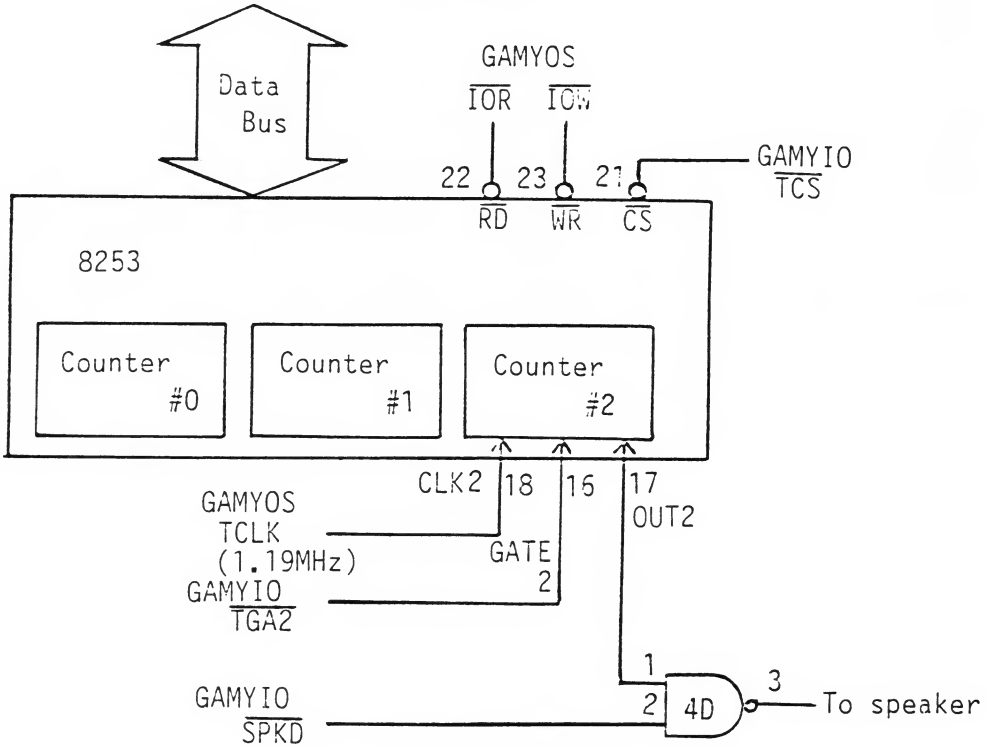
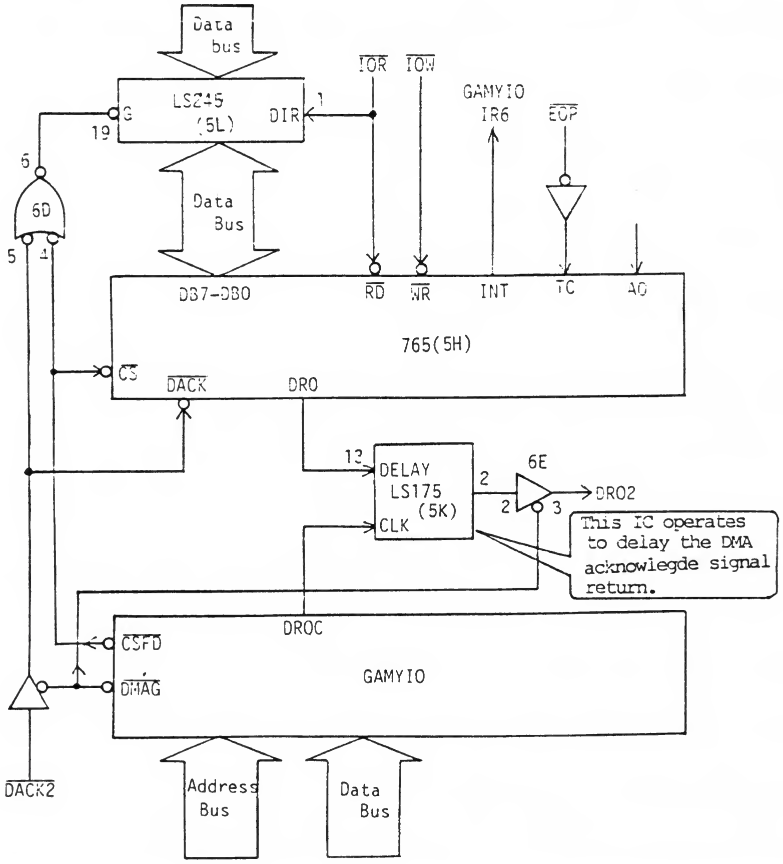


FIGURE 2-55. SPEAKER CONTROL CIRCUIT

2.2.10 **Floppy Disk Drive Control Circuit** (Figures 2-56 through 2-61)

The floppy disk drive control circuits consists of two special ICs, as shown in Figure 2-56. Table 2-11 lists the functions of these devices.



This IC operates to delay the DMA acknowiegde signal return.

FIGURE 2-56. FDD CONTROL CIRCUIT

TABLE 2-11. FDD CONTROL CIRCUIT IC FUNCTIONS

IC NAME	LOCATION	FUNCTION
FDC (uPD765AC)	5H	This IC sends control signals to each controller IC by receiving FDD command data from the CPU. It performs serial-to-parallel conversion of the data read from the FDD and parallel-to-serial conversion of data to be written. This device interfaces the CPU with the FDD control block.
GAMYIO	4K	This IC is located between the FDC and FDD. It directly controls the FDD by receiving control signals from the FDC.
VFO (SED9420CAA)	7D	This IC filters the clock bits from the FDD data read and sends only valid data to the FDC.

CPU --> FDC

The data transmission sequence between the CPU and the FDC is described below.

(1) Setting of the I/O register in the GAMYIO

The CPU sets two I/O registers in the GAMYIO with address/data bus and bus status signals. The following data is sent to these I/O registers.

I/O Register **H

* Selection of the drive A-D
* Reset of the FDC
* Mask for the DMA request
* ON/OFF control for the drive motor A-D

I/O Register **H

* Selection of the drive type (8 inch,5 inch)
* Selection of the rotation speed for the drive motor
* Disk change signal

(2) Setting of the FDC internal register

In order to set the FDC, the GAMYIO decodes the address bus and supplies the active $\overline{\text{CSFD}}$ signal.

(3) Requesting of the INT and the DRQ signal

Command Read/Write Mode

In the FDC INT mode, the FDC outputs an INT request signal to the CPU by each one byte data transmission. After receiving the INT request signal, the CPU excutes the interrupt routine, and after finishing the data transmission, the CPU outputs the INT request signal. In the DMA mode, the FDC outputs the DRQ request signal by each one byte data transmission. After finishing the DMA transmission, the CPU outputs the INT request signal.

Seek Recalibrate Mode

The FDC outputs the INT request signal after finishing the command excution.

Sequence Interrupt Status Mode

After executing the command, the CPU outputs the INT request signal.

FDC --> FDD

This section describes the operation of the FDD control.

(1) Read/Write signal
(2) Other control signals

(1) Read/Write signal

Figure 2-57 diagrams the FDD read/write signal control circuit. The FDD write signal is directly output from the FDC. The FDD read signal is input to the FDC from the FDD via the VFO IC.

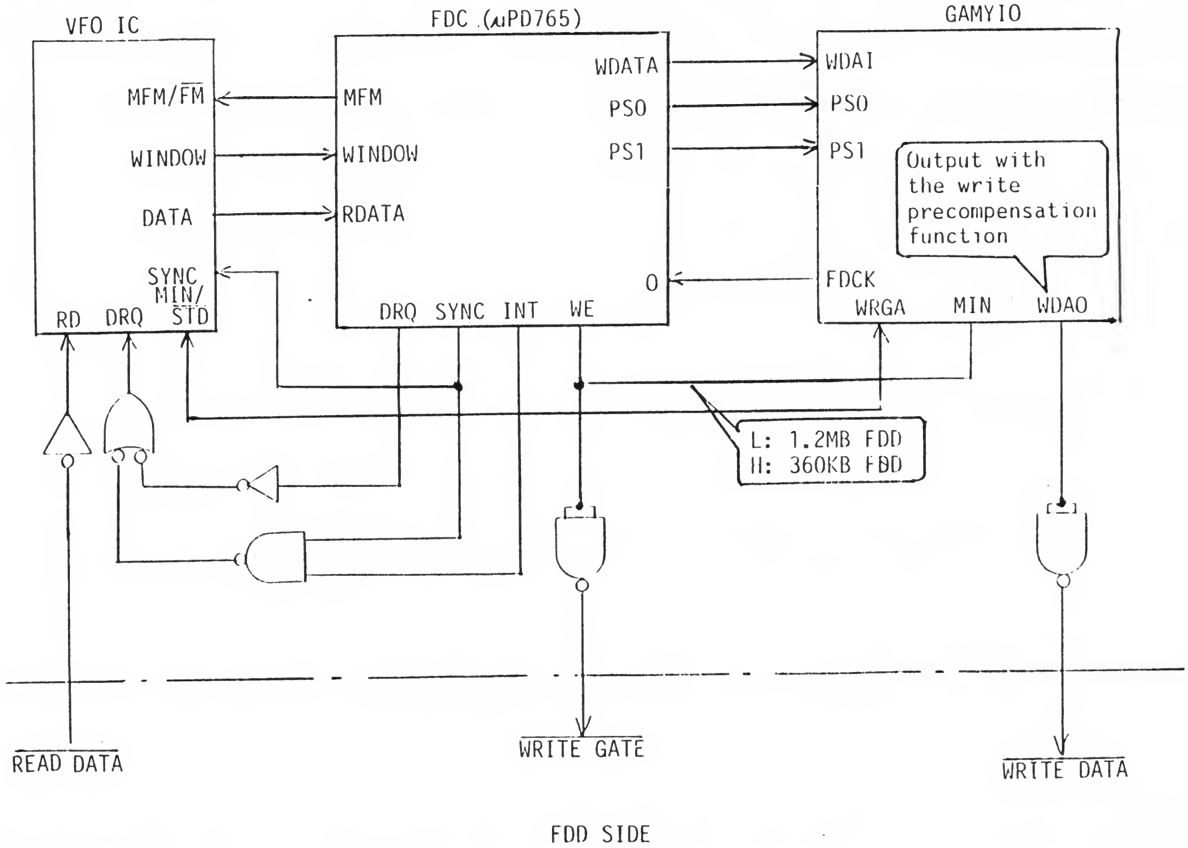


FIGURE 2-57. FDD READ/WRITE SIGNAL CONTROL CIRCUIT

Write Precompensation Circuit

The write data (WD) output by FDC is converted to MFM data. However, it is not practical to send this data directly to an FDD because peak shift error occurs. To prevent peak shift, the write data (WE) output timing is adjusted by the data write circuit, called a write precompensation circuit.
The floppy disk magnetic inversion spacing is 200 ns, 300 ns, and 400 ns. The output waveforms, with which 1 pulse is written to disk, are as shown in Figure 2-58 (left). When 2 pulses are written within 200 ns spacing, each independent waveform interfaces, the peak of the synchronous waveform is shifted from the write location as shown in Figure 2-58 (right). This is called peak shift To eliminate this interface as much as possible, write compensation is performed. Since peak shift can be foreseen, write timing is shifted in a direction which automatically reduces the peak shift. Write compensation is performed past the cylinder 128 circumference with 13 ns as required compensation. This circuit is called a write precompensation circuit and is shown in Figure 2-59.

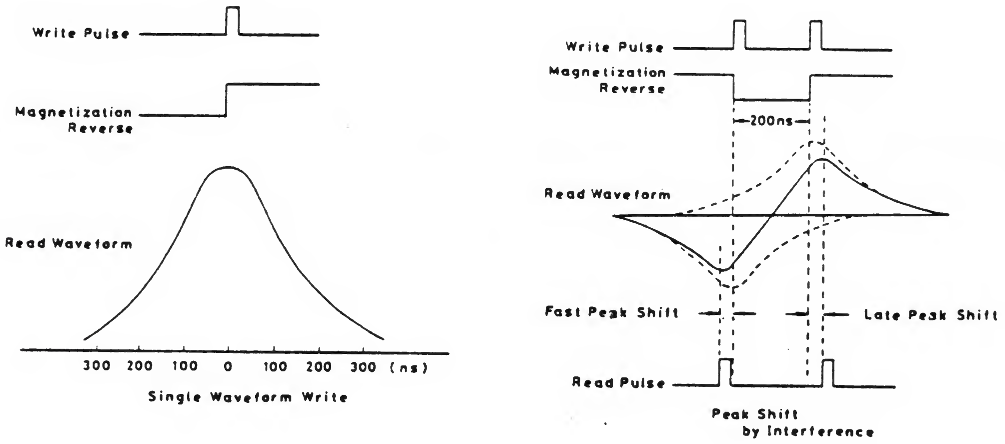


FIGURE 2-58. WRITE PRECOMPENSATION

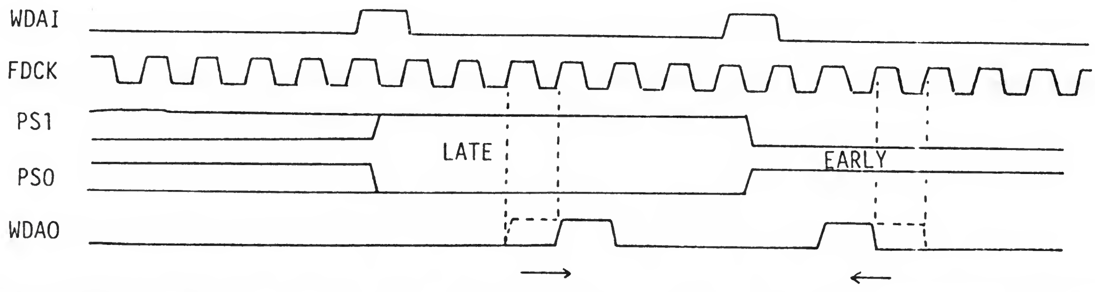


FIGURE 2-59. WRITE PRECOMPENSATION CIRCUIT

Table 2-12 shows the function of the write precompensation circuit by the combination of signals PS0 and PS1. Discrimination between ID field and DATA field Figure 2-60 shows the timing diagram for the ID field and DATA field. These signals are input to the DRQ terminal of the VFO IC from the FDC. The VFO terminal function is shown in Table 2-13.

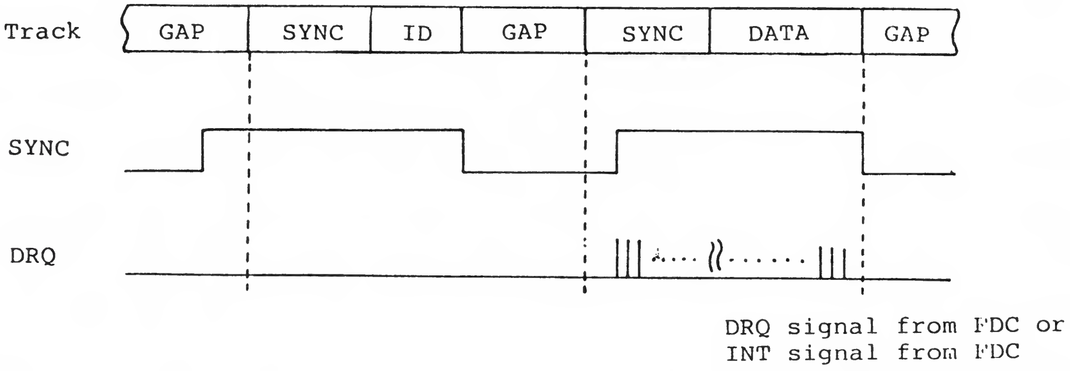


FIGURE 2-60. TIMING DIAGRAM FOR ID AND DATA FIELD

TABLE 2-12. COMBINATION OF PS0 AND PS1

PS0	PS1	SHIFT DIRECTION
0	0	Not Shifted
0	1	Backward
1	0	Forward
1	1	Invalid

TABLE 2-13. VFO TERMINAL FUNCTIONS

SIGNAL NAME	PIN NO.	I/O	FUNCTION
XG	1	I	16 MHz clock input.
ϕ1	3	O	1 MHz clock output to the 765FDC.
FDDATA	5	I	Data read from a disk drive (via the HA16642).
WINDOW	6	O	Window signal to filter-out clock bits from raw data. Supplied to the 765 FDC.
DATA	7	O	Signal wave of data to the 765 FDC.
MFM/FM	8	I	Recording method selection. Note that MFM method is set in this system using pull-up resister R83 (33 ohm).
MIN/STD	9	I	Always high level to maintain a consistent driving speed for the 3.5 inch disk.
CONTROL	11	I	Control voltage input to the internal circuit of the VFO.
OFFSET	12	I	Offset input to set the frequency of the VFO.
WCLK	14	O	Clock for the 765 FDC for writing data (1 MHz square wave).
ϕ2	15	o	Clock output to the GAMYIO (1 MHz square wave).

Figure 2-61 diagrams the internal circuit block diagram of the VFO.

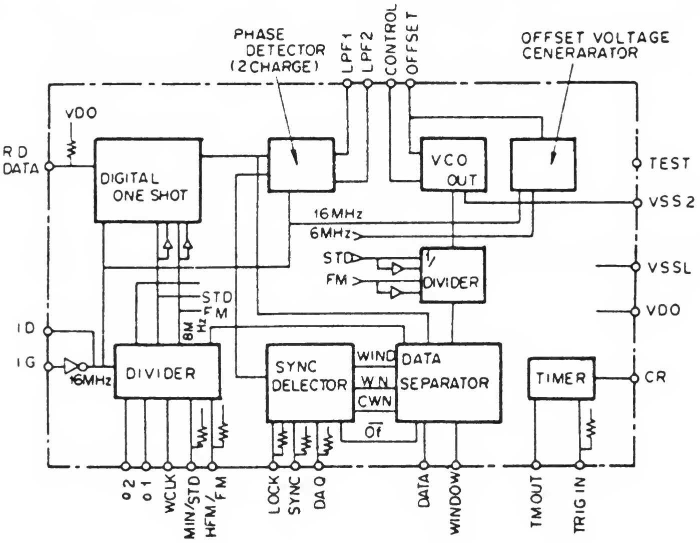


FIGURE 2-61. VFO INTERNAL CIRCUIT BLOCK DIAGRAM

Other Control Signals

Mode Signal

This signal is used for the selection signal whether the FDD type is double-density or high density.

TABLE 2-14. MOTOR ROTATION SPEED

MODE SIGNAL	MODE	MOTOR ROTATION SPEED
Low	Double density	300 rpm
High	High density	360 rpm

Disk Change Signal

This signal is supplied from the FDD. At power ON or when the diskette is removed, this signal becomes low. The signal remains low level until the following conditions are fulfilied:

(1) Diskette is inserted and the push button is depressed.
(2) Drive is selected and the step pulse is supplied.

2.2.11 **Dip SW Status Reading** (Figures 2-62 and 2-63)

Two DIP switches are located on the MCY main control board. Each DIP SW (1 and 2) is allocated as I/O port 062H and 11B6H, respectively.

DIP SW 1

Figure 2-62 diagrams the DIP SW1 status reading circuit. This circuit is included in the GAMYMC. The CPU reads the I/O register twice, four bits at a time.

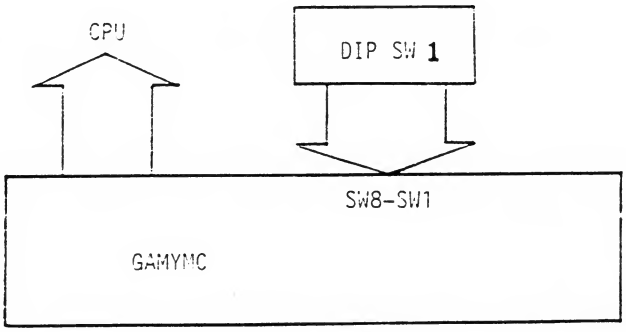


FIGURE 2-62. DIP SW 1 STATUS READING CIRCUIT

DIP SW 2

To read the status of DIP SW2, the GAMYIO receives the IOR signal and the 11B6H address; it then supplied the $\overline{\text{DPSW}}$ signal to the gate terminal of the LS245.

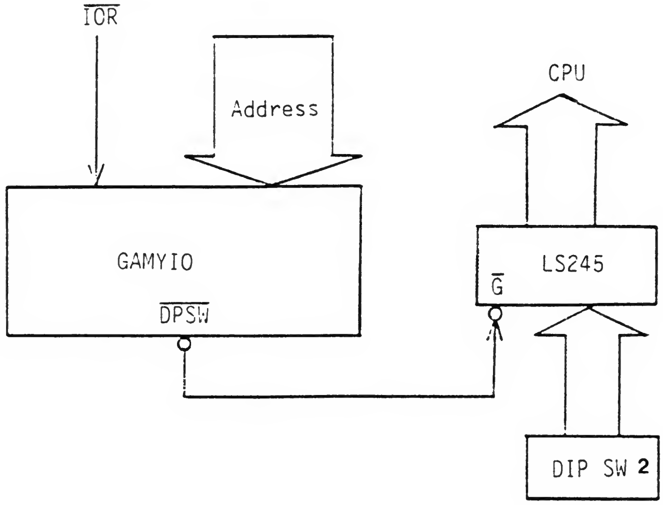


FIGURE 2-63. DIP SW 2 STATUS READING CIRCUIT

2.2.12 Keyboard Interface Circuit (Figure 2-64)

The GAMYOS controls the keyboard interface. Figure 2-64 diagrams the keyboard interface circuit and Table 2-15 shows the pin function of the keyboard interface connector.

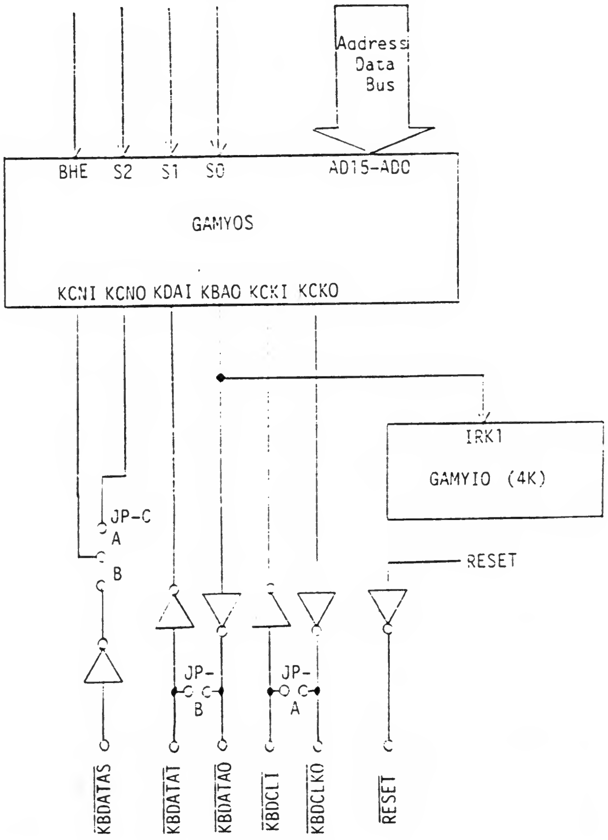


FIGURE 2-64. KEYBOARD INTERFACE CIRCUIT

TABLE 2-15. PIN FUNCTION OF KEYBOARD INTERFACE

PIN NO.	SIGNAL	I/O	FUNCTION
1	KBDCLK	I/O	Keyboard clock signal. Supplied from PB6 of 82C55 (17E).
2	KBDDATA	I/O	Keyboard data line. The serial data from the keyboard is input.
3	KBDRST	O	Keyboard reset signal. Supplied with the system reset signal on MARS board.
4	KBDGND	-	Keyboard ground line. Connected to ground on MARS board.
5	KBD+5	-	Keyboard power supply (+5 V).
6	KBDCNT	I/O	Indicates the CPU does not receive the transmit data from the keyboard.
7	KBDSRP	I	Indicates nine-bit data are transmitted from the keyboard.
8	KBDTST	I/O	When this line is low for 10 ms, keyboard automatically excutes by itself, if the keyboard is normal, data AAH is output from the keyboard, and if abnormal, data 80H is output.

Table 2-16 shows the jumper settings for use with the EPSON and IBM keyboard. ⟨B⟩

TABLE 2-16. KEYBOARD JUMPER SETTING

JP	EPSON	IBM
A	Short	Short
B	Open	Short
C	Short B side	Short A side

2.3 MCYPSE Power Supply Operation (Figure 2-65)

B

The power supply section, which consists of the primary side board (MCYPS-AC) and the secondary side board (MCYPS-DC-E) of the transformer, and provides DC voltages of +5V, -5V, +12V, -12V, and non-switched +5V. The MCYPS-DC-E board includes two custom ICs for the switching reguration, four series regulators, a voltage sensing circuit, and a software power switching control circuit. Figure 2-65 is a power supply block diagram.

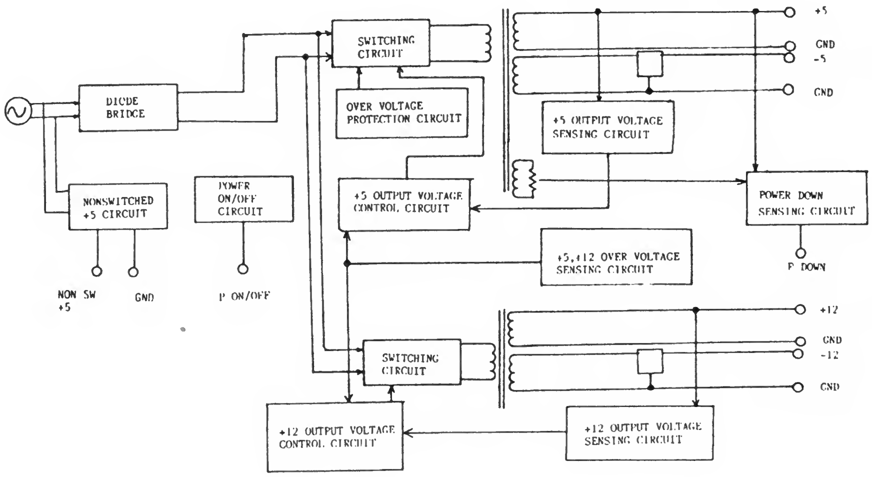

SWITCHING CIRCUIT
DICDE BRIDCE
OVER VOLTAGE PROTECTION CIRCUIT
+5 OUTPUT VOLTAGE SENSING CIRCUIT
+5
GND
-5
GND
NONSWITCHED +5 CIRCUIT
POWER ON/OFF CIRCUIT
+5 OUTPUT VOLTAGE CONTROL CIRCUIT
POWER DOWN SENSING CIRCUIT
+5,+12 OVER VOLTAGE SENSING CIRCUIT
P DOWN
NON SW +5
GND
P ON/OFF
+12
GND
-12
GND
SWITCHING CIRCUIT
+12 OUTPUT VOLTAGE CONTROL CIRCUIT
+12 OUTPUT VOLTAGE SENSING CIRCUIT

FIGURE 2-65. POWER SUPPLY BLOCK DIAGRAM

2.3.1 General Specifications (Figure 2-66)

INPUT VOLTAGE	AC 120 V (AC85-132V)
FREQUENCY	49-61 Hz
INPUT CURRENT	1.7A (Typ.)
INPUT SERGE CURRENT	32A (Max.)
FUSE	125 V 6.3A
INSULATION STRENGTH	AC 1000 V for 1 minute between the primary and the secondary side. AC 500V for 1 minute between the secondary side and F.G.
INSULATION RESISTANCE	50M ohms for 500 VDC minimum.

TABLE 2-17. POWER SUPPLY SPECIFICATIONS

OUTPUT VOLTAGE	+5 V	+12 V	-12 V	-5 V	NS+5 V
Output voltage	5.0 V ±5%	12.0 V ±5%	-12.0 V ±10%	-5.0 V ±10%	5.0 V ±5%
Output current (Typ.)	7.5A	4.7A	0.3A	0.3A	0.02A
Minimum output current	1A	0.32A	0A	0A	0.01A
Ripple voltage	50 mV	100 mV	100 mV	50 mV	100 mV
Overcurrent protection circuit	7 V	16.8 V	-	-	-

Output Sequence

+5V and 12V output is switched by the POWER-ON/OFF signal.

"H" level ----- ON

Power Down Signal

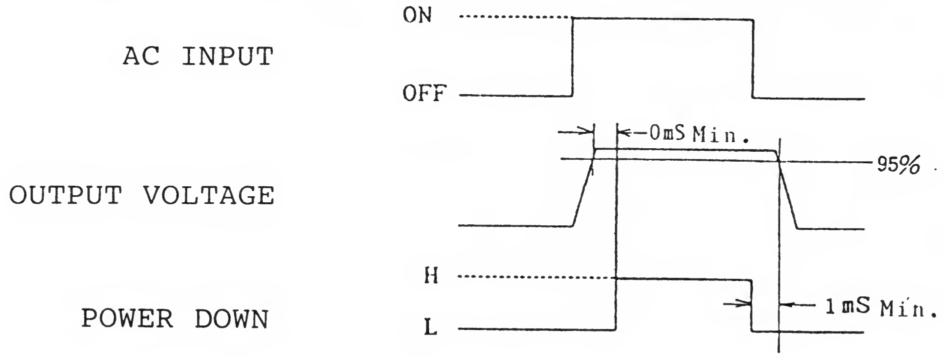


FIGURE 2-66. POWER DOWN SIGNAL

2.3.2 MCYPSE (Power Supply) Unit

2.3.2.1 Basic Circuit (Figures 2-67 and 2-68)

Figure 2-67 shows the basic circuit of the MCYPSE power supply unit. The switching method is applied for the rectification. The switching oscillation is controlled by the current io.

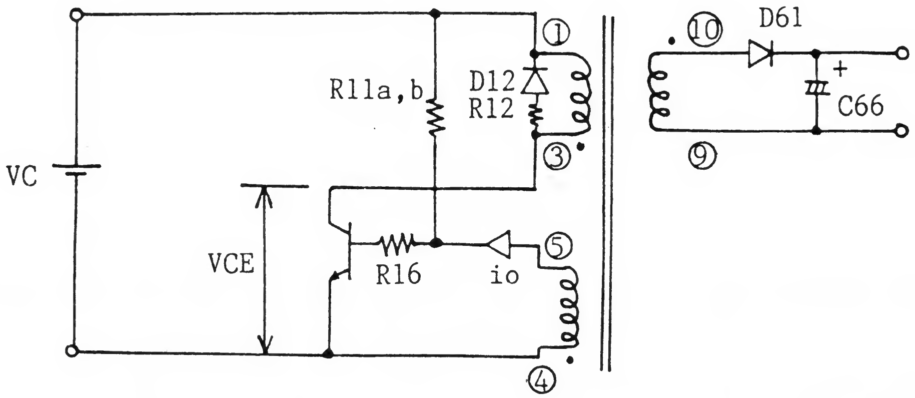


FIGURE 2-67. BASIC CIRCUIT

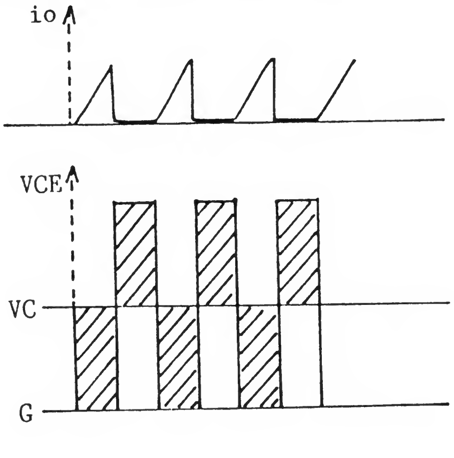


FIGURE 2-68. SWITCHING WAVEFORM

2.3.2.2 Protection Circuit (Figures 2-69 through 2-71)

(1) When the voltage between pin 4 and pin 5 of the TP1 increases more than 5.1V, the transistor TrA turns to off.

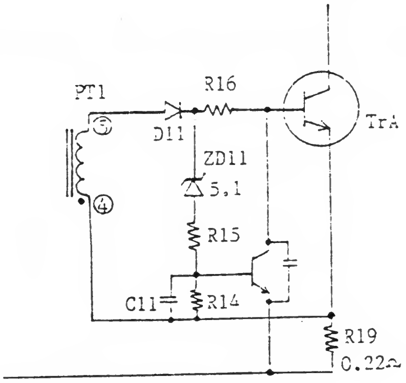


FIGURE 2-69. PROTECTION CIRCUIT 1

(2) When the voltage between Ⓟ and Ⓠ is conductive by the PC1 and the PC2, the transistor TrA and TrB turn to on, and then the base current of the transistor TrC will be not supplied.

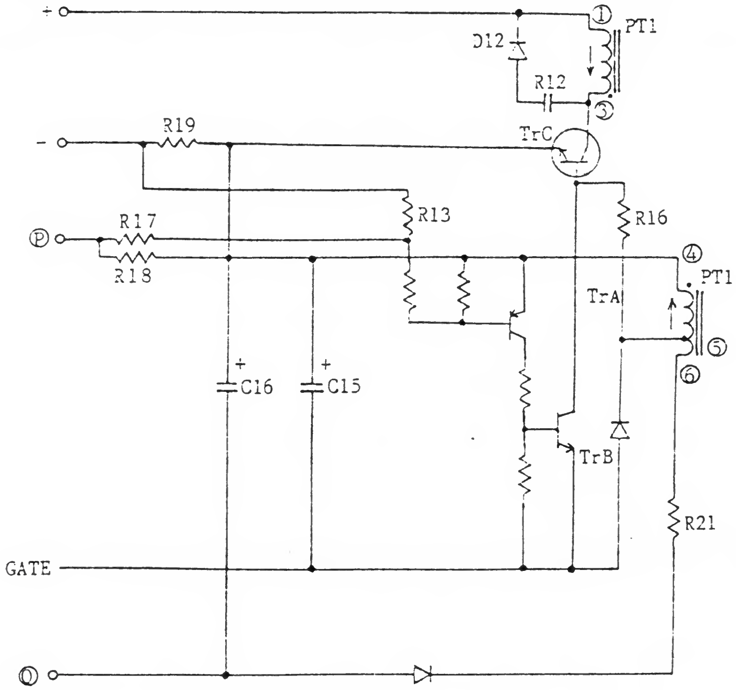


FIGURE 2-70. PROTECTION CIRCUIT 2

(3) Power Down Detect Circuit

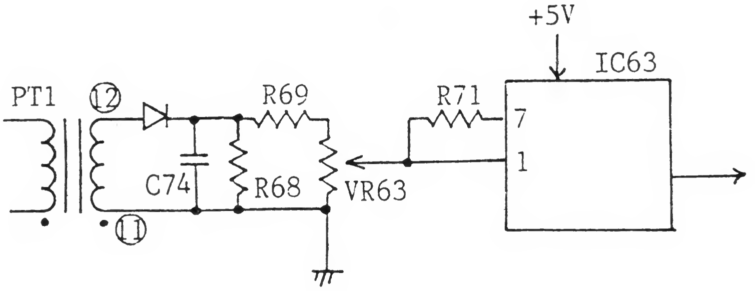


FIGURE 2-71. POWER DOWN DETECT CIRCUIT

(4) Overcurrent Protection Circuit

Zenor diode ZD63, ZD64 are used for the overcurrent detection for the +5V and +12V lines.

2.3.2.3 Software Power Switching Control Circuit (Figure 2-72)

Figure 2-72 shows the power switching control circuit by software on the MCYPSE-AC-A. When the high level switching control signal is input, the power is supplied to the diode D1, and the system will be powered up.

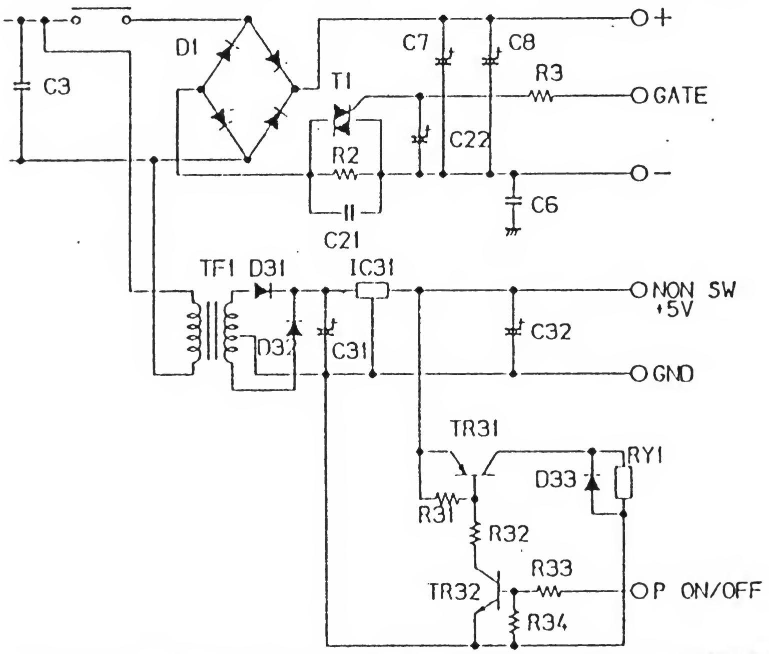


FIGURE 2-72. SOFTWARE POWER SWITCHING CONTROL CIRCUIT

CHAPTER

3

OPTIONS

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3.2 MCY-RA BOARD 3-2

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3-2 MCY-RA Connector Pin Assignments 3-5

3.1 MCY-MT (MOTHER) BOARD (Figure 3-1)

The MCY-MT mother board has five option slots. Figure 3-1 shows the circuit diagrams of the MCY-MT board and Table 3-1 describes the pin assignments for the option slot interface connectors.

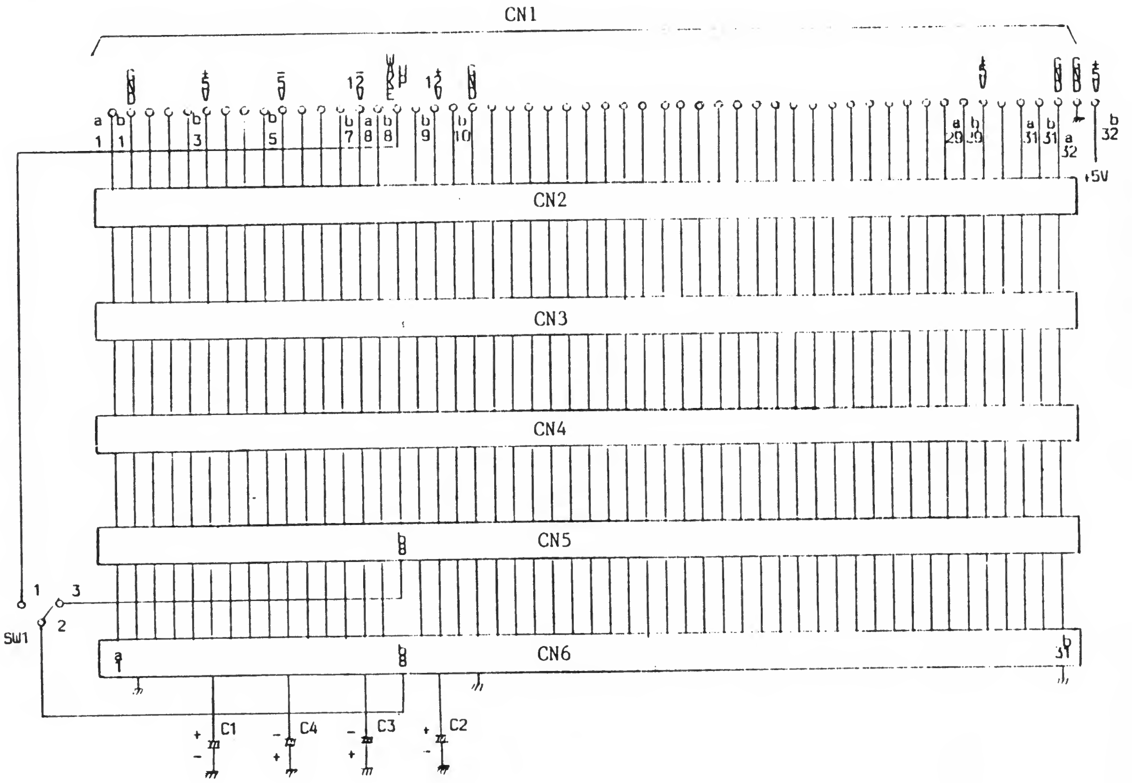

FIGURE 3-1. MCY-MT BOARD CIRCUIT DIAGRAM

Tables 3-1 describes the pin assignments for the option slot interface connectors.

TABLE 3-1. CN2, CN3, CN4 AND CN5 PIN ASSIGNMENTS

PIN NO.	SIGNAL NAME	DIRECTION	FUNCTION
A1	$\overline{\text{IOCHCK}}$	I	I/O Check; provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.
A2	D7	I/O	Data Bit 7
A3	D6	I/O	Data Bit 6
A4	D5	I/O	Data Bit 5
A5	D4	I/O	Data Bit 4
A6	D3	I/O	Data Bit 3
A7	D2	I/O	Data Bit 2
A8	D1	I/O	Data Bit 1
A9	D0	I/O	Data Bit 0
A10	IOCHRDY	I/O	I/O Check Ready; is used for any slow device to drive it low immediately upon detecting its valid address and a R/W command.
A11	AEN	O	Address Enable; is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place When this line is active, the DMA controller has control of the address bus, the memory data-bus and I/O.
A12	A19	O	Address Bit 19
A13	A18	O	Address Bit 18
A14	A17	O	Address Bit 17
A15	A16	O	Address Bit 16
A16	A15	O	Address Bit 15
A17	A14	O	Address Bit 14
A18	A13	O	Address Bit 13
A19	A12	O	Address Bit 12
A20	A11	O	Address Bit 11
A21	A10	O	Address Bit 10
A22	A9	O	Address Bit 9
A23	A8	O	Address Bit 8
A24	A7	O	Address Bit 7
A25	A6	O	Address Bit 6
A26	A5	O	Address Bit 5
A27	A4	O	Address Bit 4
A28	A3	O	Address Bit 3
A29	A2	O	Address Bit 2
A30	A1	O	Address Bit 1
A31	A0	O	Address Bit 0
A32	GND	-	Ground

B1	GND	-	Ground
B2	RESETDRV	O	Reset, used to reset or initialize system logic at PWD signal active.
B3	N.C.	-	Unused
B4	IRQ 2	I	Interrupt Request 2
B5	-5 V	I	-5 V Mother Board Power
B6	DRQ 2	I	DMA Request 2
B7	-12 V	-	-12 V Mother Board Power
B8 (*)	N.C.	-	Unused
B9	+12 V	-	+12 V Mother Board Power
B10	GND	-	Ground
B11	$\overline{\text{MEMW}}$	O	Memory Write
B12	$\overline{\text{MEMR}}$	O	Memory Read
B13	$\overline{\text{IOW}}$	O	I/O Write
B14	$\overline{\text{IOR}}$	O	I/O Read
B15	$\overline{\text{DACK 3}}$	O	DMA Acknowledge 3
B16	DRQ 3	I	DMA Request 3
B17	$\overline{\text{DACK 1}}$	O	DMA Acknowledge 1
B18	DRQ 1	I	DMA Request 1
B19	$\overline{\text{DACK 0}}$	O	DMA Request 0
B20	CLOCK	O	4.772 MHz CPU Clock
B21	IRQ 7	I	Interrupt Request 7
B22	IRQ 6	I	Interrupt Request 6
B23	IRQ 5	I	Interrupt Request 5
B24	IRQ 4	I	Interrupt Request 4
B25	IRQ 3	I	Interrupt Request 3
B26	$\overline{\text{DACK 2}}$	O	DMA Acknowledge 2
B27	T/C	O	DMA Terminal Count
B28	ALE	O	Address Latch Enable
B29	N.C.	-	Unused
B30	OSC	O	14.318 MHz Oscillator Clock
B31	GND	-	Ground
B32	N.C.	-	Unused

NOTE: The B8 of the CN6 is only connected to WAKE UP signal from the MCY main
(*) control board.

3.2 MCY-RA BOARD (Figure 3-2)

The MCY-RA board is configured with four 4 x 64 bit DRAMs, and is used for expanding the main memory capacity. It is possible to expand the main memorx up/to 640K bytes using the MCY-RA board. Figure 3-2 diagrams the MCY-RA board, and Table 3-2 describes the pin assignments of connector CN1 on the MCY-RA board. ⟨B⟩

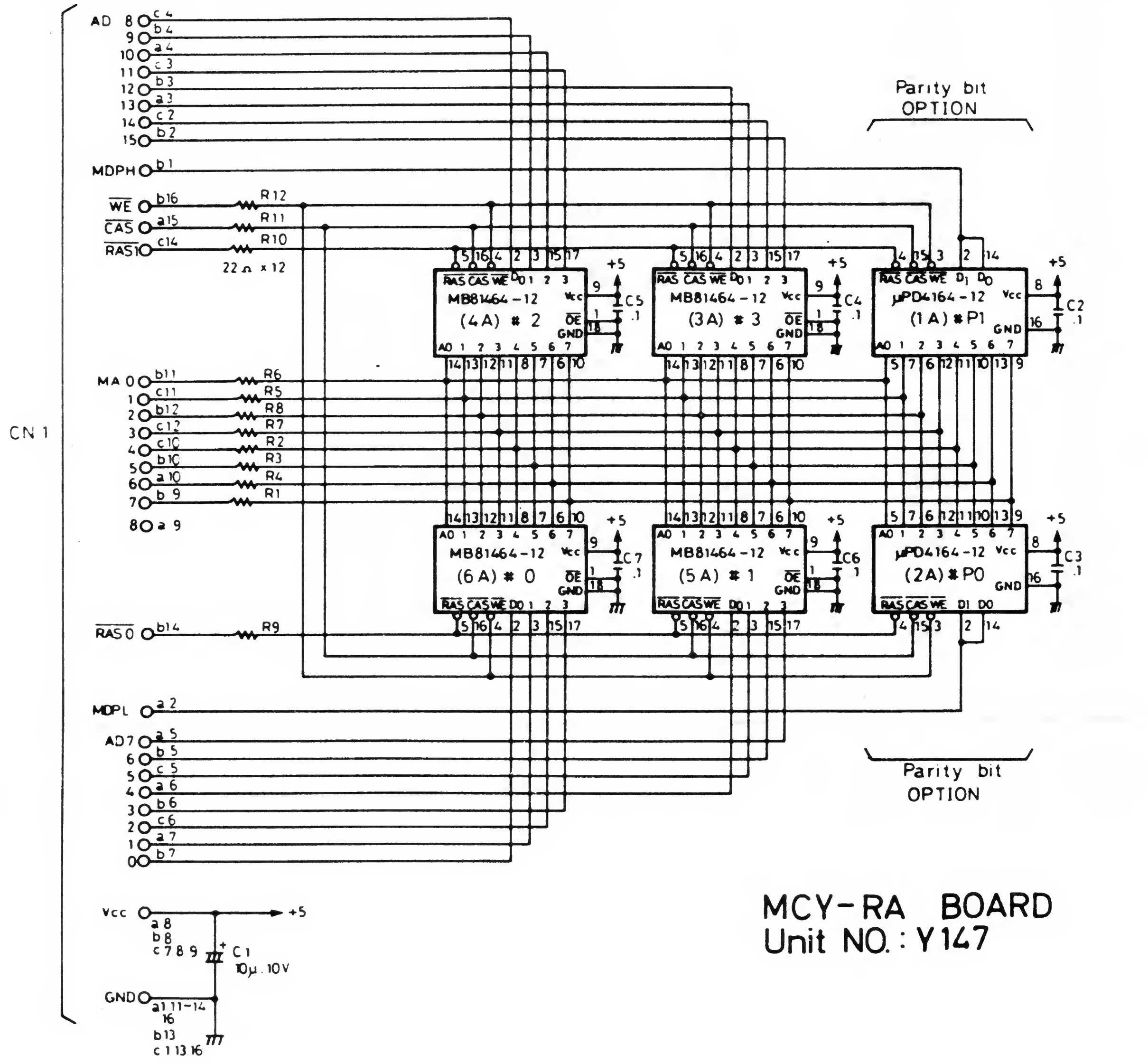

FIGURE 3-2. MCY-RA BOARD CIRCUIT DIAGRAM

The memory chips that are applicable to the expansion RAM are:

FUJITSU MB81464-12

TABLE 3-2. CN1 (MCY-RA BOARD) PIN ASSIGNMENTS

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
A1	GND	-	Ground
A2	MDPL	O	Parity Low Bits
A3	AD13	I/O	Address & Data Bit 13
A4	AD10	I/O	Address & Data Bit 10
A5	AD7	I/O	Address & Data Bit 7
A6	AD4	I/O	Address & Data Bit 4
A7	AD1	I/O	Address & Data Bit 1
A8	+5 V	-	+5 V
A9	MA8	O	Memory Address Bit 8
A10	MA6	O	Memory Address Bit 6
A11	GND	-	Ground
A12	GND	-	Ground
A13	GND	-	Ground
A14	GND	-	Ground
A15	$\overline{\text{CAS}}$	O	Colume Address Storbe
B1	MDPH	I/O	Parity High Bits
B2	AD15	I/O	Address & Data Bit 15
B3	AD12	I/O	Address & Data Bit 12
B4	AD9	I/O	Address & Data Bit 9
B5	AD6	I/O	Address & Data Bit 6
B6	AD3	I/O	Address & Data Bit 3
B7	AD0	I/O	Address & Data Bit 0
B8	+5 V	-	+5 V
B9	MA7	O	Memory Address Bit 7
B10	MA5	O	Memory Address Bit 5
B11	MA0	O	Memory Address Bit 0
B12	MA2	O	Memory Address Bit 2
B13	GND	-	
B14	$\overline{\text{RAS0}}$	O	Row Address Strobe 0
B15	RAS2	O	Row Address Strobe 2
B16	$\overline{\text{WE}}$	O	Write Enable
C1	GND	-	
C2	AD14	I/O	Address & Data Bit 14
C3	AD11	I/O	Address & Data Bit 11
C4	AD8	I/O	Address & Data Bit 8
C5	AD5	I/O	Address & Data Bit 5
C6	AD2	I/O	Address & Data Bit 2
C7	+5 V	-	+5 V
C8	+5 V	-	+5 V
C9	+5 V	-	+5 V
C10	MA4	O	Memory Address Bit 4
C11	MA1	O	Memory Address Bit 1
C12	MA3	O	Memory Address Bit 3
C13	GND	-	Ground
C14	$\overline{\text{RAS1}}$	O	Row Address Strobe 1
C15	RAS3	O	Row Address Strobe 3
C16	GND	-	Ground
A16	GND	-	Ground

NOTE: Signal direction is as viewed from the MCY-RA board.

CHAPTER

4

TROUBLESHOOTING

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4.1 MODULAR TROUBLESHOOTING

Modular troubleshooting enables isolation of malfunctions of the items listed in Table 4-1. Table 4-3 lists tools necessary for modular testing. Table 4-4 is a troubleshooting reference guide for determing malfunction boards according to malfunction symptom.

note : Units received from the field should be carefully inspected for signs of misuse or shipping damage. Note the packing materials used to ship the system, if applicable, and look for protective apacers between the read/write heads and for the shipping support at the option port.

TABLE 4-1. MODULAR SUBASSEMBLIES

NAME	MODEL	IC LOCATION	Q'TY	PART NUMBER
CPU's	uPD70116	1Q	1	X400071160
GAMYMC	E01064EA	7L	1	X147800401
GAMYDM	E01063EA	4N	1	Y147800301
GAMYVD GAMYVA	E02052EA E02051EA	2D	1	Y147800601 Y147800501
GAMYOS	E01062EA	3N	1	Y147800201
GAMYIO	E01061EA	4K	1	Y147800101
DMA Controller	8237	4Q	1	X400082374
Read Time Clock	146818	7C	1	X400014680
CRT Controller	MB89322	2H	1	X400893221
Main Memory	MB81256-10	8H 8J-8N 8P,8Q 9H 9J-9N 9P,9Q	16	X400582561
Video Memory	MB81416-10	3C-3F 3H,3J 2K,3L	1	X400084161

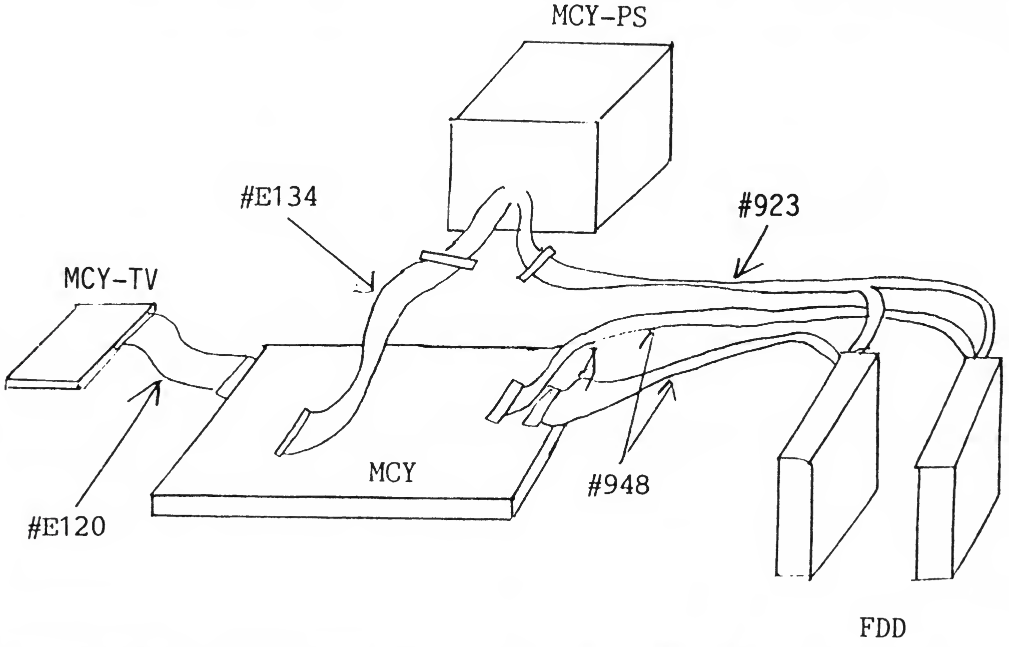

FIGURE 4-1. EXTENSION CABLE CONNECTIONS

TABLE 4-2. EXTENSION CABLES

TOOL NO.	PART NO.	DESCRIPTION
# 948	Y130312000	Connection between the MCY board and the FDD signal line.
# 923	Y116320000	Connection between the MCY-PS unit and the FDD power line.
# E134	B777601901	Connection between the MCY board and the MCY-PS unit.
# E120	B777601201	Connection between the MCY board and the MCY-MT board.

TABLE 4-3. MODULAR TROUBLESHOOTING TOOLS

TOOL	PART NUMBER
Phillips screwdriver (#1)	B743800100
Digital VOM	----------
System disk (MS-DOS)	----------
Blank disk	----------

TABLE 4-4. TROUBLESHOOTING REFERENCE GUIDE

SYMPTOM	PROBABLE CAUSE
System does not boot	**MCYPSE** Unit (Power supply unit) MCY Board (Main control board)
FDD does not Read/Write	FDD Unit MCY Board MCY-PS Unit DIP SW Mis-setting (Refer to 7.1) Floppy Disk Mis-using
Display malfunction	MCY Board Monitor DIP SW Mis-setting (Refer to 7.1)
RS-232C does not operate	MCY Board DIP SW Mis-setting (Refer to 7.1)
Not print out	MCY Board DIP SW Mis-setting (Refer to 7.1)
Speaker does not beep	Speaker MCY Board
Keyboard does not input	Keyboard MCY Board
Option Card does not operate	Option Card MCY Board Jumper Mis-setting (Refer to 7.2)
Can not be turned power on/off	**MCYPSE** Unit MCY Board

Table 4-5 is the troubleshooting reference guide for determing malfunction ICs on the MCY main control board according to malfunction symptom, and Table 4-6 is described for the **MCYPSE** power supply unit troubleshooting.

TABLE 4-5. MCY BOARD TROUBLESHOOTING REFERENCE GUIDE

SYMPTOM	PROBABLE CAUSE DEVICE	DESCRIPTION
System does not boot	CPU uPD70116/V30 (7Q) ROM 2764 (4U,5U) DRAM MB81256 (9Q,H,J,K,L,M,N,P 8Q,H,J,K,L,M,N,P) GAMYMC (7L) GAMYOS (3N)	*CPU clock *Reset signal *PROM select signal *RAS,CAS signal *DRAM referesh *ALE signal
FDD does not Read/Write	VFO SED9420CAC (7D) DMAC (4Q) GAMYDM (4N) GAMYIO (4K)	*WINDOW signal *CS signal of FDC *DREQ signal *FDD control signal (MOTOR ON, DRIVE SELECT.....)
	GAMYOS (3N)	*IOW,IOR signal of FDC
Display Malfunction	GAMYVD (2D) GAMYVA (1L) VRAM MB81416 (3C,E,H,K,D,F,J,L) GDC MB89322B (2H)	
RS-232C does not operate	GAMYIO (4K) GAMYOS (3N)	*Interrupt Request signal of RS-232C *INTA signal
Not print out	GAMYIO (4K) GAMYOS (3N)	*Interrupt Request signal of printer *INTA signal
Speaker does not Beep	8253 (2T) GAMYOS (3N) GAMYIO (4K)	*Frequency Generator *Clock for the 8253 *TGA2 signal of 823 *SPKD sigal *CS signal for the 8253
Keyboard does not input	GAMYOS (3N) GAMYIO (4K)	*Interrupt Request signal of keyboard
Option card does not operate	8237 (4Q) GAMYDM (4N) GAMYOS (3N) GAMYIO (4K)	*Interrupt Request

B

TABLE 4-6. **MCYPSE** UNIT TROUBLESHOOTING REFERENCE GUIDE

SYMPTOM	DEVICE
Non-SW+5 is not supplied	IC31 (L78M05)
At power up, R2 is birnt	T1 (DTA10E or G) IC11, IC 12 (STK7360) C15 (47uF/16V)
Power is not turned on/off	Tr31,32 (2SB544, 2SC1570) RY1
Output voltage is not supplied	IC11,12 (STK7360) PC1, PC2 (PC713) C16, C46 (22uF/50V) PR1 (S22MD1)
Power down signal is output at operation	IC63 (MB3761) VR63 Mis-adjustment (detected at 78VAC) TR61 (2SC1570)

CHAPTER

5

DISASSEMBLY AND ASSEMBLY

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5.1 GENERAL REPAIR INFORMATION

This section provides procedures for removal and replacement of the major subassemblies of EQUITY II, and includes a list of tools with EPSON part numbers. These tools are also commercially available.

TABLE 5-1. REPAIR TOOLS AND EQUIPMENT

TOOLS	PART NUMBER
Phillips screwdriver (#1)	B743800100
Phillips screwdriver (#2)	B743800200
E-ring holder (#2.5)	B740800400
E-ring holder (#1.5)	B740800200
Torque driver	B740100102
Tweezers	B741000100
Hex unit driver	----------
Soldering iron	B740200100

DANGER

THE MONITOR IN THIS SYSTEM INCLUDES HIGH VOLTAGE CIRCUITRY. DISCONNECT THE MONITOR FROM THE AC OUTLET BEFORE DISASSEMBLY. IMMEDIATELY AFTER REMOVING THE MONITOR CASE, USE A SCREWDRIVER OR SIMILAR DEVICE TO SHORT THE ANODE OF THE CART TO THE CONDUCTIVE CABLE ON THE TUBE. DO NOT ATTEMPT TO DISCHARGE THE ANODE BY CONNECTING IT WITH ISOLATED PARTS OF THE MONITOR, AS THIS MAY PRODUCE A SHOCK HAZARD.

WARNING

The circuit boards contain static-sensitive CMOS IC and must be handled with care. Discharge bodily static before removing circuit boards, and wear a grounded wrist strap during disassembly. Place the boards on rubber mats or similar non-static surfaces when they are removed from the case.

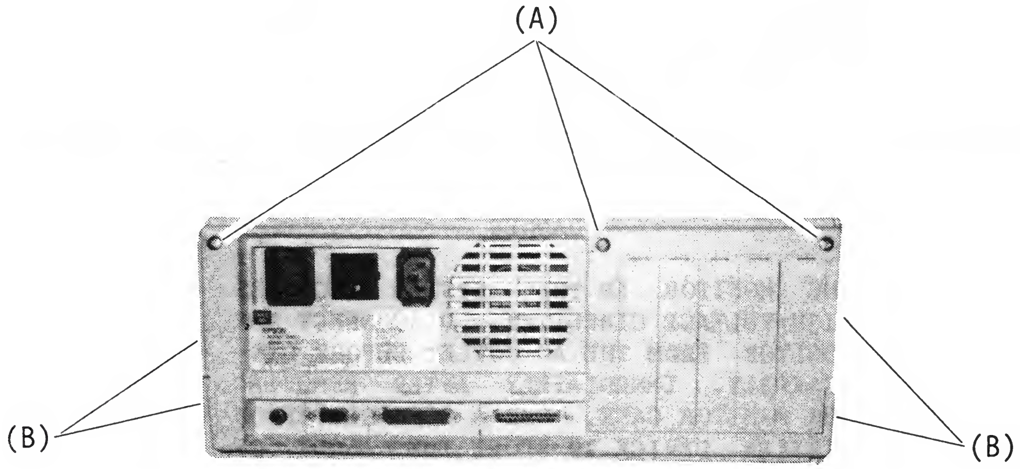
5.2 MAIN UNIT DISASSEMBLY AND ASSEMBLY

5.2.1 Rear Panel and Upper Case Removal (Figure 5-1)

1. Remove three screws (A) from the rear panel, and pull the panel from the main unit.

2. Remove screw covers on the right side of the panel.

3. Remove four screws (B) and lift the upper case straigh up.



NOTE: This is a picture of the EQUITY II.
EPSON PC+ has only one AC outlet. B

FIGURE 5-1. REAR PANEL AND UPPER CASE REMOVAL/REPLACEMENT

5.2.2 Rear Panel and Upper Case Replacement (Figure 5-1)

1. Install the upper case in the main unit, and secure the case with four screws (B).

2. Install the rear panel in the main unit, and secure the panel with three screws (A).

NOTE: Make sure that tabs (C) in the rear panel is fitted into the lower case.

5.2.3 Front Panel Removal (Figure 5-2)

1. Remove the rear panel. (Section 5.2.1)
2. Remove the upper case. (Section 5.2.1)
3. Remove four screws (A) from the front panel.
4. Disconnect connector (B).
5. Remove tab (C) in the front panel which is fitted to the lower case, and remove the front panel.

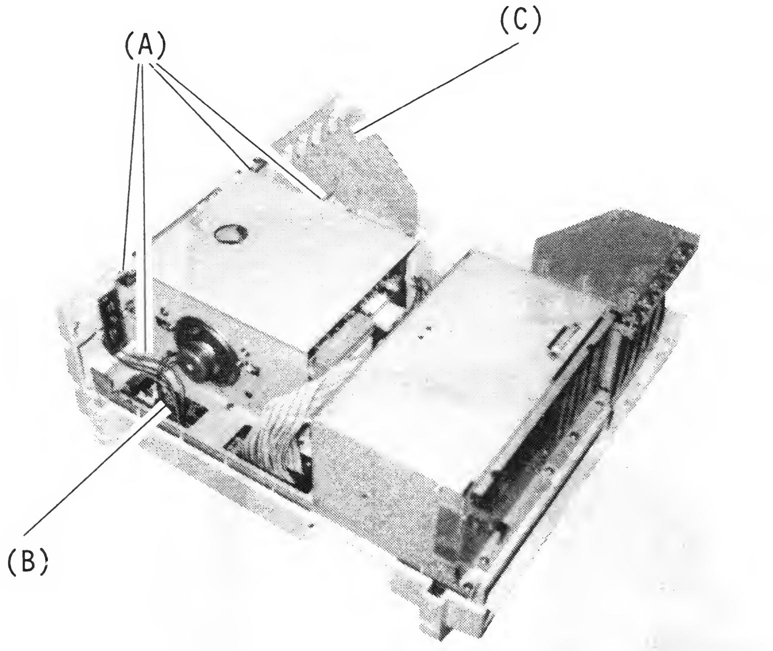


FIGURE 5-2. FRONT PANEL REMOVAL/REPLACEMENT

5.2.4 Front Panel Replacement (Figure 5-2)

1. Install the front panel in the lower case.

NOTE: Make sure that tab (C) in the rear panel is fitted into the lower case.

2. Secure the front panel with four screws (A), and connect connector (B).
3. Install the upper case. (Section 5.2.2)
4. Install the rear panel. (Section 5.2.2)

5.2.5 Option Card Removal (Figure 5-3)

1. Remove the rear panel. (Section 5.2.1)

2. Remove the upper case. (Section 5.2.1)

3. Remove screw (A) which secures the option card.

4. Lift the option card straight up.

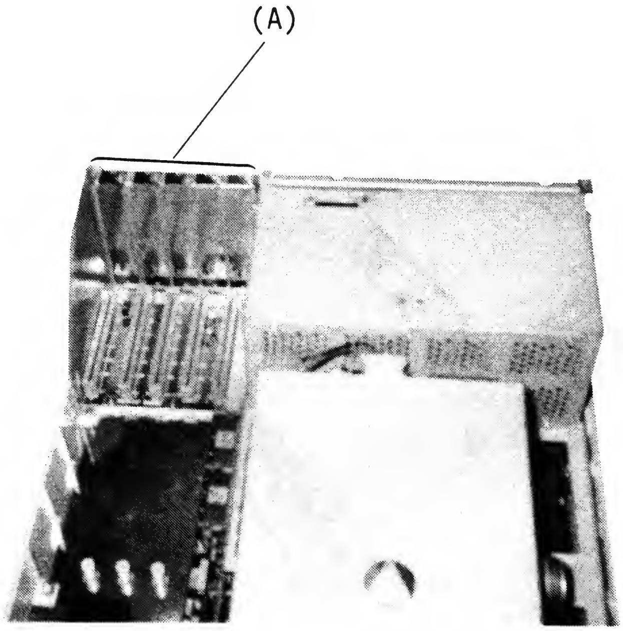


FIGURE 5-3. OPTION CARD REMOVAL/REPLACEMENT

5.2.6 Option Card Replacement (Figure 5-4)

1. Install the option card in any option slot.

2. Tighten screw (A) to secure the option card.

3. Install the upper case. (Section 5.2.2)

4. Install the rear panel. (Section 5.2.2)

5.2.7 MCYPSE Power Suuply Unit Removal (Figure 5-4)

B

1. Remove the rear panel. (Section 5.2.1)

2. Remove the upper case. (Section 5.2.1)

3. Remove three screws (A) which secure the MCYPSE power supply unit.

4. Disconnect three connectors (B).

5. Lift the power supply unit from the lower case.

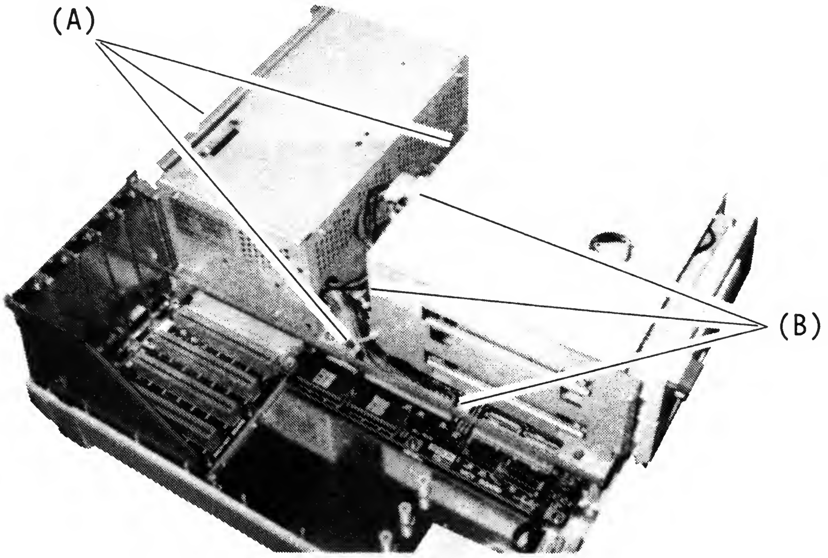


FIGURE 5-4. MCYPSE POWER SUPPLY UNIT REMOVAL/REPLACEMENT

5.2.8 MCYPSE Power Supply Unit Replacement (Figure 5-4)

1. Install the power supply unit in the lower case.

2. Secure the unit with three screws (A), and connect three connectors (B) to the MCY board.

3. Install the upper case. (Section 5.2.2)

4. Install the rear panel. (Section 5.2.2)

5.2.9 MCY-MT Mother Board Removal (Figure 5-5)

1. Remove the rear panel. (Section 5.2.1)
2. Remove the upper case. (Section 5.2.1)
3. Remove the option card. (Section 5.2.5)
4. Remove four screws (A) from the MCY-MT mother board.
5. Remove the mother board from the lower case.

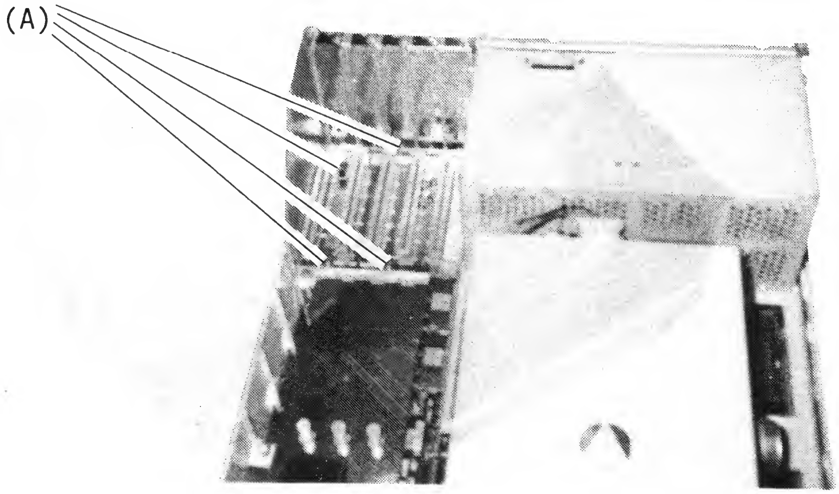


FIGURE 5-5. MCY-MT MONITOR BOARD REMOVAL/REPLACEMENT

5.2.10 MCY-MT Mother Board Replacement

1. Install the mother board in the lower case.
2. Secure the mother board with four screws (A).
3. Install the option card. (Section 5.2.6)
4. Install the upper case. (Section 5.2.2)
5. Install the rear panel. (Section 5.2.2)

5.2.11 MCY Main Control Board Removal (Figure 5-6)

1. Remove the rear panel. (Section 5.2.1)
2. Remove the upper case. (Section 5.2.1)
3. Remove the front panel. (Section 5.2.3)
4. Remove eight screws (A) which secure frame (E) to the lower case, and disconnect four connectors (B).
5. Remove three screws (C) and then remove the frame (D).
6. Remove frame (E) which includes the FDD units and the power supply unit.
7. Remove the MCY-MT mother board. (Section 5.2.9)
8. Disconnect connector (G) from the litium battery.
9. Remove nine screws (F) which secure the MCY board.
10. Lift the MCY board straight up.

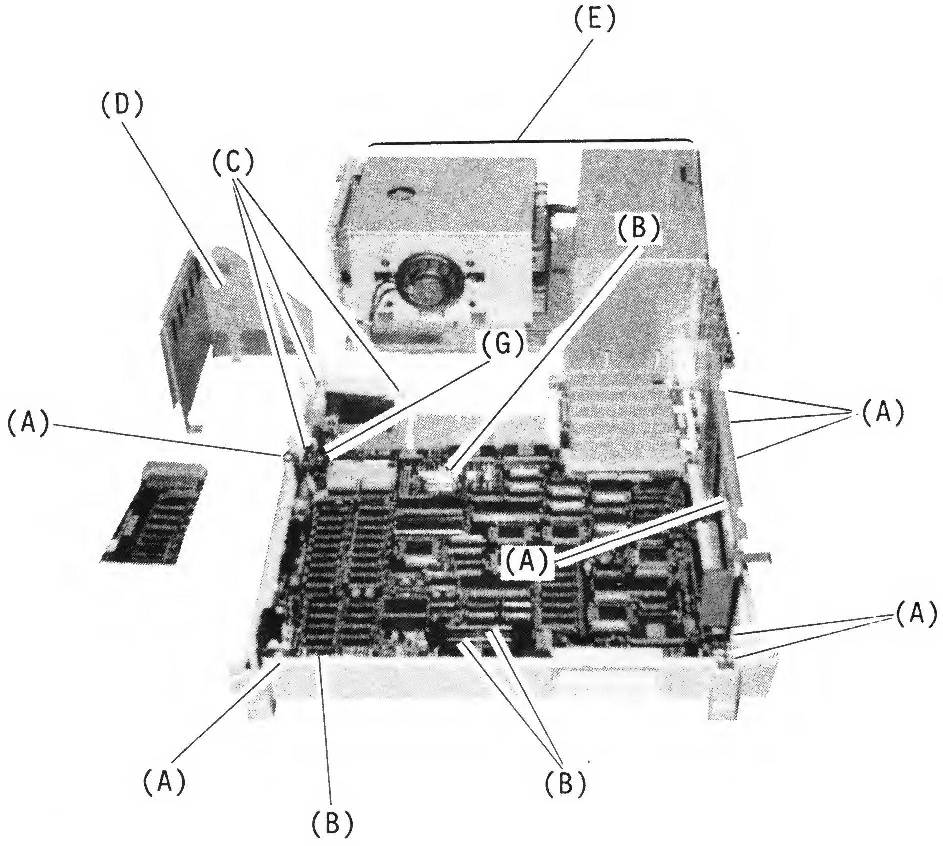


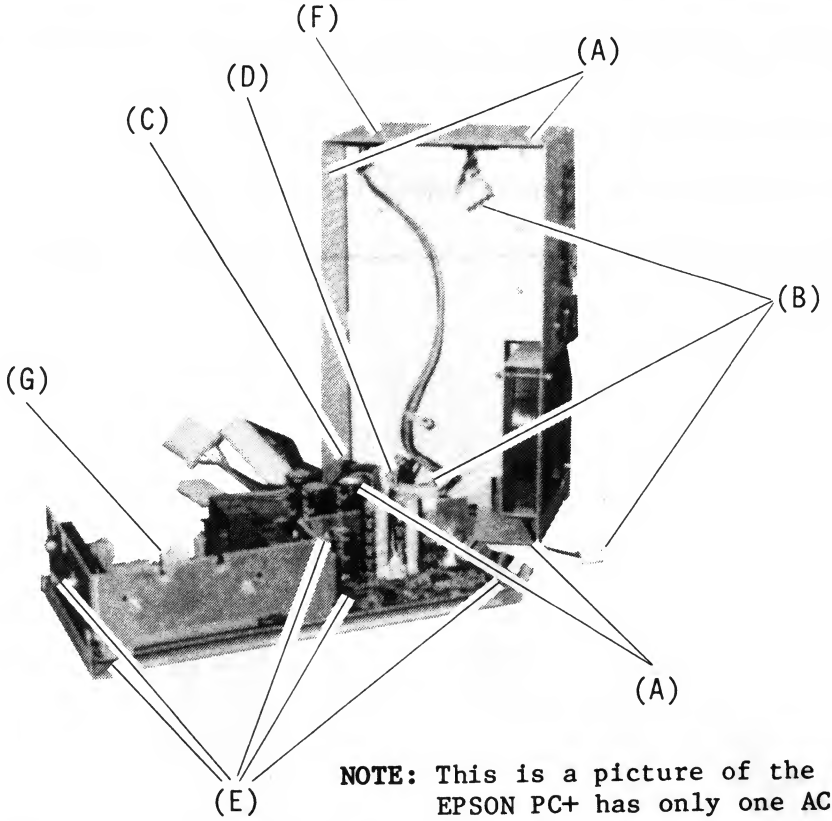
FIGURE 5-6. MCY MAIN CONTROL BOARD REMOVAL/REPLACEMENT

5.2.12 MCY Main Control Board Replacement (Figure 5-6)

1. Install the MCY main control board in the lower case and secure the board with nine screws (F).
2. Connect connector (G).
3. Install the MCY-MT board. (Section 5.2.10)
4. Secure frames (D) and (E) with three screws (C) and eight screws (A), respectively.
5. Connect four connectors (B).
6. Install the front panel. (Section 5.2.4)
7. Install the upper case. (Section 5.2.2)
8. Install the rear panel. (Section 5.2.2)

5.2.13 MCYPSE Secondary Side Board Removal (Figure 5-7)

1. Remove the MCYPSE power supply unit from the lower case. (Section 5.2.7) ⟨B]
2. Remove four screws (A), from the power supply unit and disconnect three connectors (B).
3. Push down (Release) tab (C) with a screwdriver and remove cable (D) from power supply chasis (F).
4. Remove six screws (E) from the secondary side board (G) and lift the circuit board straight up.



NOTE: This is a picture of the EQUITY II. EPSON PC+ has only one AC outlet.

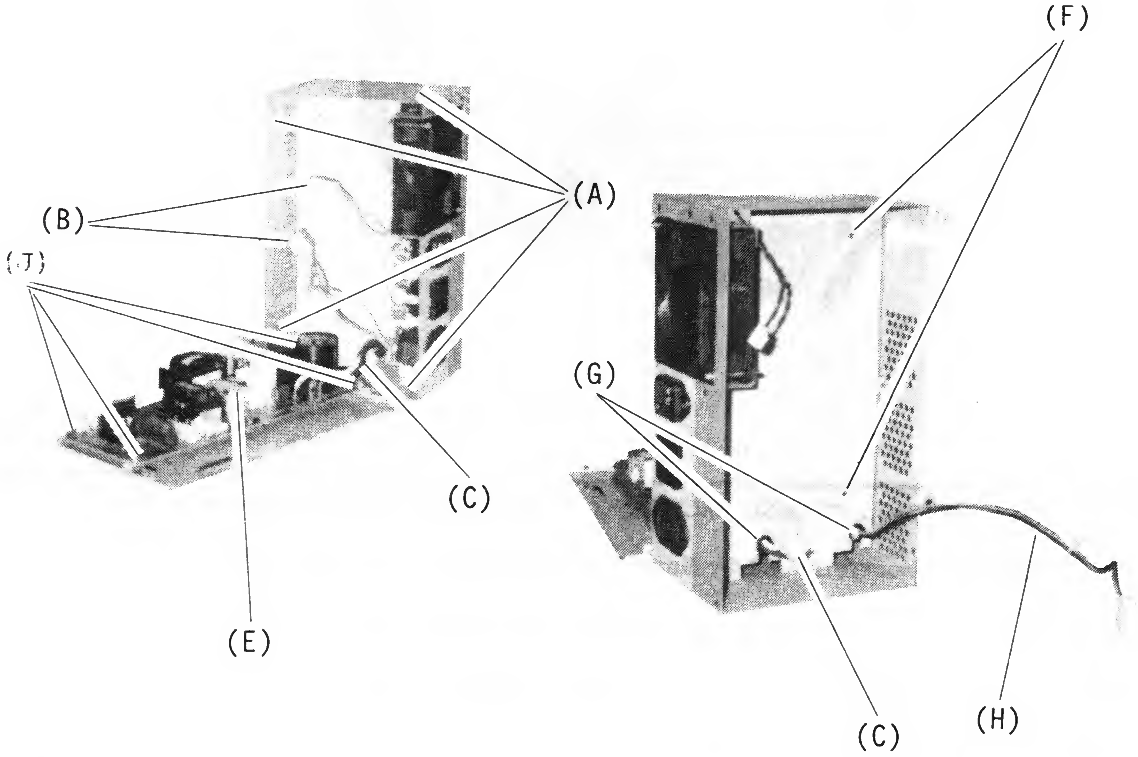
FIGURE 5-7. MCYPSE SECONDARY SIDE BOARD REMOVAL/REPLACEMENT

5.2.14 MCYPSE Secondary Side Board Replacement (Figure 5-7)

1. Install the circuit board (G) with six screws (E).
2. Secure cable (D) to the power supply chassis (F).
3. Connect three connectors (B).
4. Secure the circuit board with four screws (A).
5. Install the power supply unit in the lower case. (Section 5.2.8)

5.2.15 MCYPSE Primary Side Board Removal (Figure 5-8) B

1. Remove the secondary side board of the MCYPSE. (Section 5.2.13)
2. Remove four screws (A) from the power supply unit.
3. Remove two screws (F) from the secondary side of the MCYPSE.
4. Disconnect two connectors (B).
5. Push cable (C) to the primary side circuit board for 5 or 6 cm.
6. Remove the primary side circuit board (E) from the power supply chassis.
7. Push down (Release) tabs (G) with a flat-blade screwdriver, and remove cables (C) and (H) from the power supply board.
8. Remove four screws (J) from the circuit board.
9. Lift the primary side circuit board straight up.



NOTE: This is a picture of the EQUITY II.
EPSON PC + has only one AC outlet. B

FIGURE 5-8. MCYPSE PRIMARY SIDE BOARD REMOVAL/REPLACEMENT

5.2.16 **MCYPSE Primary Side Board Replacement** (Figure 5-9)

1. Install the primary side circuit board with four screws (J).
2. Install cables (C) and (H) to the secondary side of the MCYPSE.
3. Set tabs (G).
4. Install cables to the power supply chasis with two screws (F).
5. Connect two connectors (B).
6. Install the circuit board and the frame with four screws (A).
7. Install the secondary side circuit board. (Section 5.2.14)

5.3 FLOPPY DISK DRIVE DISASSEMBLY AND ASSEMBLY

5.3.1 FDD Unit Removal (Figure 5-11)

1. Remove the rear panel. (Section 5.2.1)
2. Remove the upper case. (Section 5.2.1)
3. Remove two screws (B) to remove drive A; remove two screws (C) to remove drive B.
4. Disconnect connectors and slide the drive through the opening in the front case of the main unit to remove.

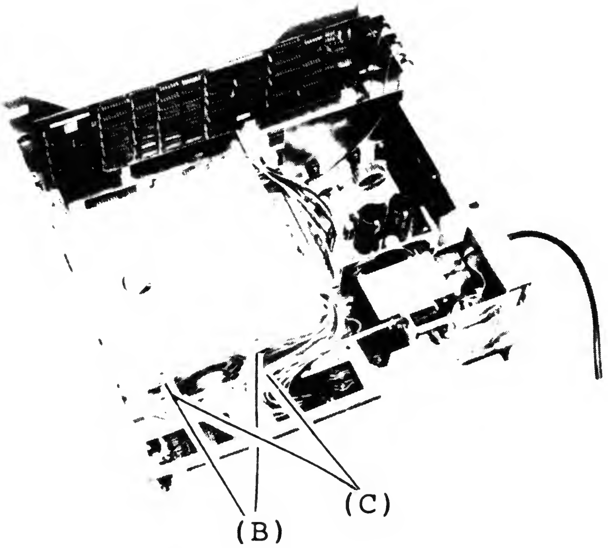


FIGURE 5-11. FDD UNIT REMOVAL/REPLACEMENT

5.3.2 FDD Unit Replacement (Figure 5-11)

1. Slide the drive through the opening in the front case. Install two screws (B) to secure drive A, and two screws (C) to secure drive B.
2. Install connectors.
3. Install the upper case. (Section 5.2.2)
4. Install the rear panel. (Section 5.2.2)

5.3.3 Main Circuit Board Removal (Figure-12)

1. Insert the point of tweezers (A) in the LED stopper (B) in the front panel gently, push the face of LED by a plastic stick (D) with taking care not to hurt. And then remove the LED from the front panel.

NOTE: Do not bent the LED stopper too much since the atopper is damaged.

2. Remove the head lead wire connector P5-J5 (E) and Index A Connector P4-J4 (F).

3. Remove set screws (G) - (I) and washer (J) securing the main circuit board assembly. (Figure 5-12)

   Set Screws M 2.5 x 6 ..... G,H
   M 2.5 x 5 I
   Toothed Washer .... J

4. Raising the main circuit board nearly in parallel with the main frame, remove the inter-board connector P3-J3 (K).

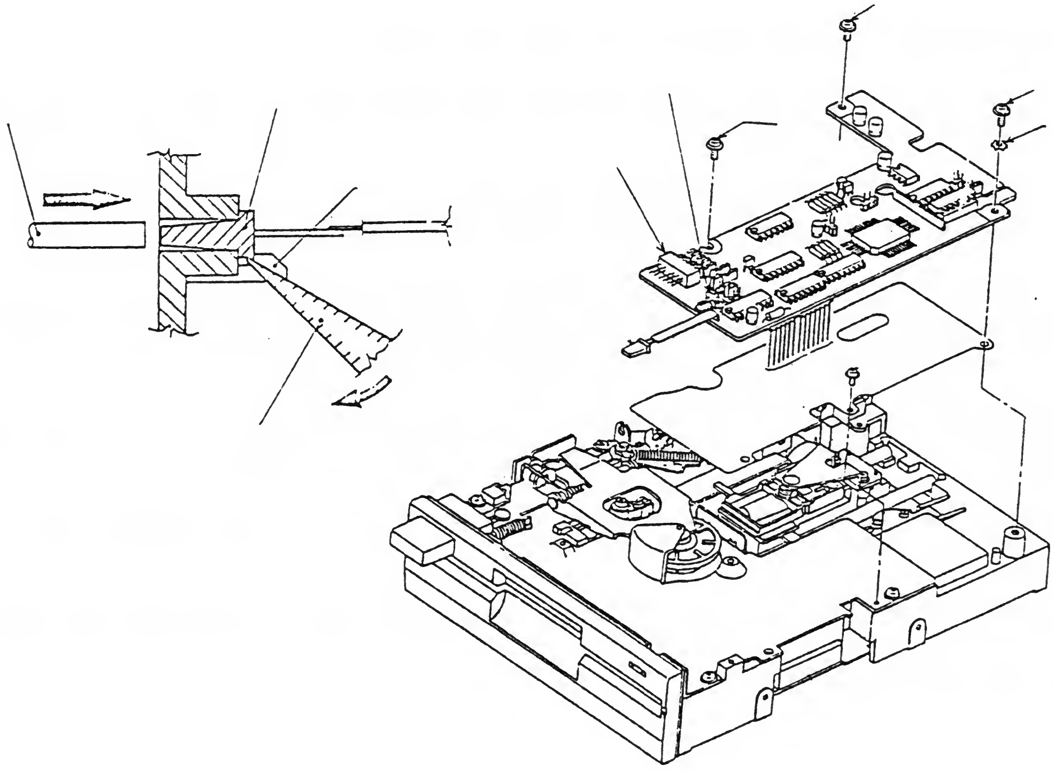


FIGURE 5-12. SD-521 MAIN CONTROL BOARD REMOVAL/REPLACEMENT

5.3.4 Main Circuit Board Replacement (Figure 5-12)

1. Cover the head lead wires with the head lead protector, and then put on the subframe.

2. Insert the board-to-board male connector (K) of the main circuit board properly into the female connector of the motor circuit board.

NOTE: Push the near of the connector.

3. Secure the main circuit board assy with the set screws and washers. (G)-(J) Screw tightning torque: 4.0 to 6.0 kg cm for A to C.

4. Connect the index load wires (F) and head lead wires (E).

5. Set the LED (C) on the front panel until this fits in the front panel.

NOTE: Take care not to deform terminals excessively in installing or removing the connectors.

5.3.5 SD-521 Front Panel, Subframe, and Collect Removal (Figure 5-13)

1. Remove the main control board. (Section 5.3.3)

2. Remove the two screws (C) which secure the front panel, and pull the panel toward front side to remove.

3. Insert a piece of papaer between the heads, remove the four screws (D) which secure the subframe unit and remove the subframe.

4. Turn the collet lever in the direction indicated by arrow (A) in Figure 5-13 to disengage the lever from the guide shaft. Move the collet in the direction indicated by arrow (B) to remove the collet set.

5. Remove the (E) ring from the collet lever shaft, disengage the collet lever spring from the hook on the subframe, and remove the shaft.

6. Remove the (E) ring from the head load fulcrum shaft, and remove the head load lever spring.

7. Disengage the head load lever fulcrum shaft and lift it from the mechanism.

8. Remove the pushbutton.

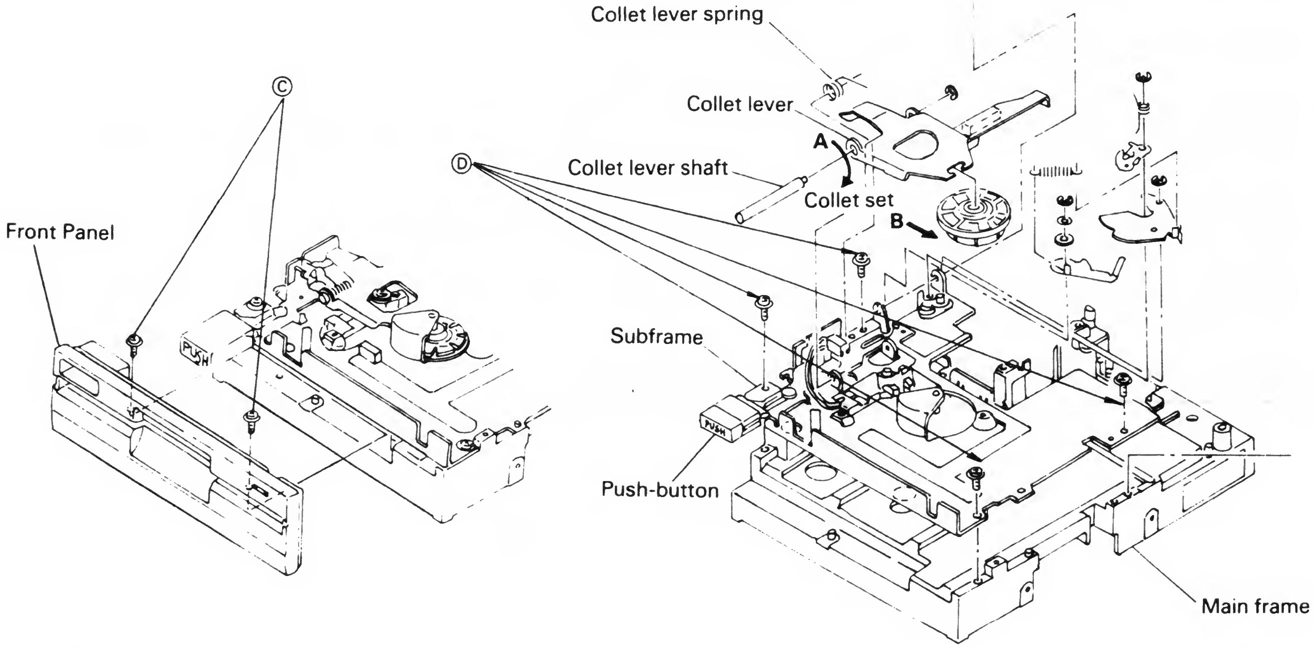


FIGURE 5-13. SD-521 FRONT PANEL, SUBFRAME AND CONTROL REMOVAL/REPLACEMENT

5.3.6 SD-521 Front Panel, Subfram and Collect Replacement (Figure 5-13)

1. Install the collet lever and collet lever spring on the subfram, and secure them with an E-ring on the collet lever shaft.
2. Turn the collet lever and position the lever end in the collet groove.
3. Align the collet center hole with the subfram guide shaft to install the collet on the subframe. Check the rotation and motion of the collet.
4. Install the head load lever and head load shaft on the subframe and secure the assembly with an E-ring. Install the head load lever so that its position corresponds with the pushbutton position.
5. Install the subframe on the main frame and secure it with four secrews (D). Use a torque drive to tighten the screws to 3.0 - 7.0 Kg/cm.
6. Install the SD-521 front panel with two screws (C).
7. Install the main control board. (Section 5.3.4)

5.3.7 Track 00 Sensor (and Jacket Lifter Spring) Removal (Figure 5-14)

1. Remove the main control board. (Section 5.3.3)
2. Remove the SD-521 front panel. (Section 5.3.5)
3. Remove the screw which secures the shield plate and remove the shield from the main board.
4. Remove the track 00 sensor connector from the motor board.
5. Remove the track 00 sensor adjustment screw (A), move the detector to the side and lift to remove.
6. Remove the jacket lifter spring, if necessary.

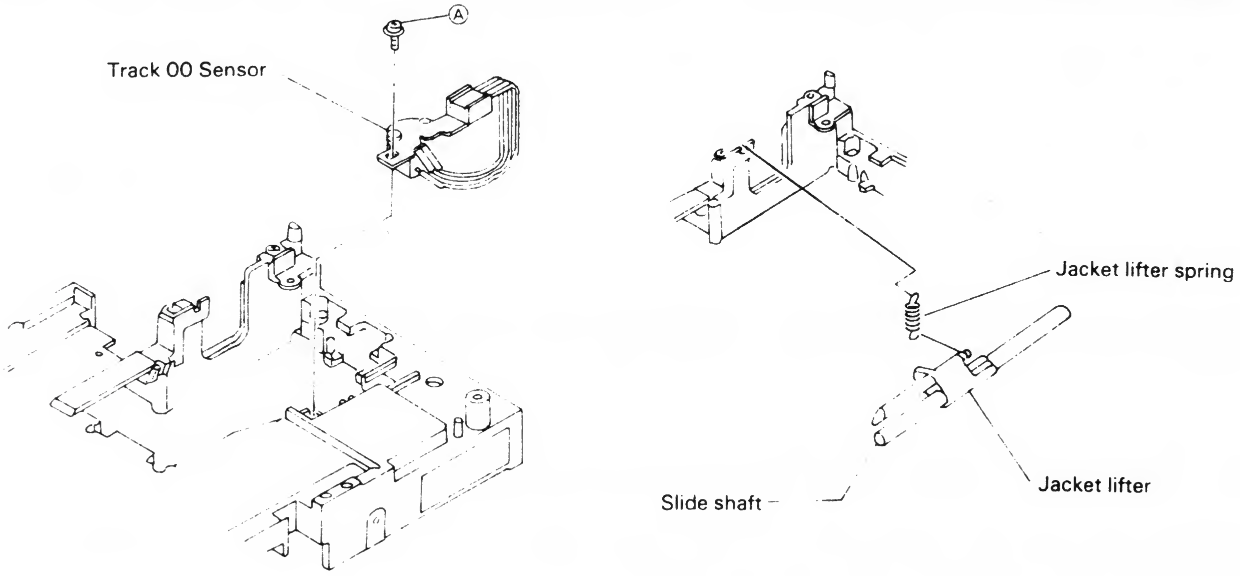


FIGURE 5-14. TRACK 00 SENSOR (AND JACKET LIFTER SPRING) REMOVAL/REPLACEMENT

5.3.8 Track 00 Sensor (and Jacket Lifter Spring) Replacement (Figure 5-14)

1. Install the jacket lifter spring on the main frame.
2. Install the track 00 sensor assembly on the main frame and temporarily tighten the adjustment screw (A).
3. Connect the track 00 connector to the motor board.
4. Install the SD-521 front panel. (Section 5.3.6)
5. Install the main control board. (Section 5.3.4)
6. Adjust the track 00 sensor.

5.3.9 Stepper Motor Removal (Figure 5-15)

1. Remove the main control board. (Section 5.3.3)
2. Remove the SD-521 front panel and subframe unit. (Section 5.3.5)
3. Remove the jackette lifter spring. (Section 5.3.7)
4. Disconnect the motor lead wires from the motor board.
5. Remove the screws (C) from the ends of the steel belt, remove the steel belt tension spring, and remove the belt from the carriage.

WARNING

Replace the belt if it becomes crimped or bent in any way during removal or replacement.

6. Remove the two screws (D) from the stepper motor mounting bracket, and lift the motor to remove.

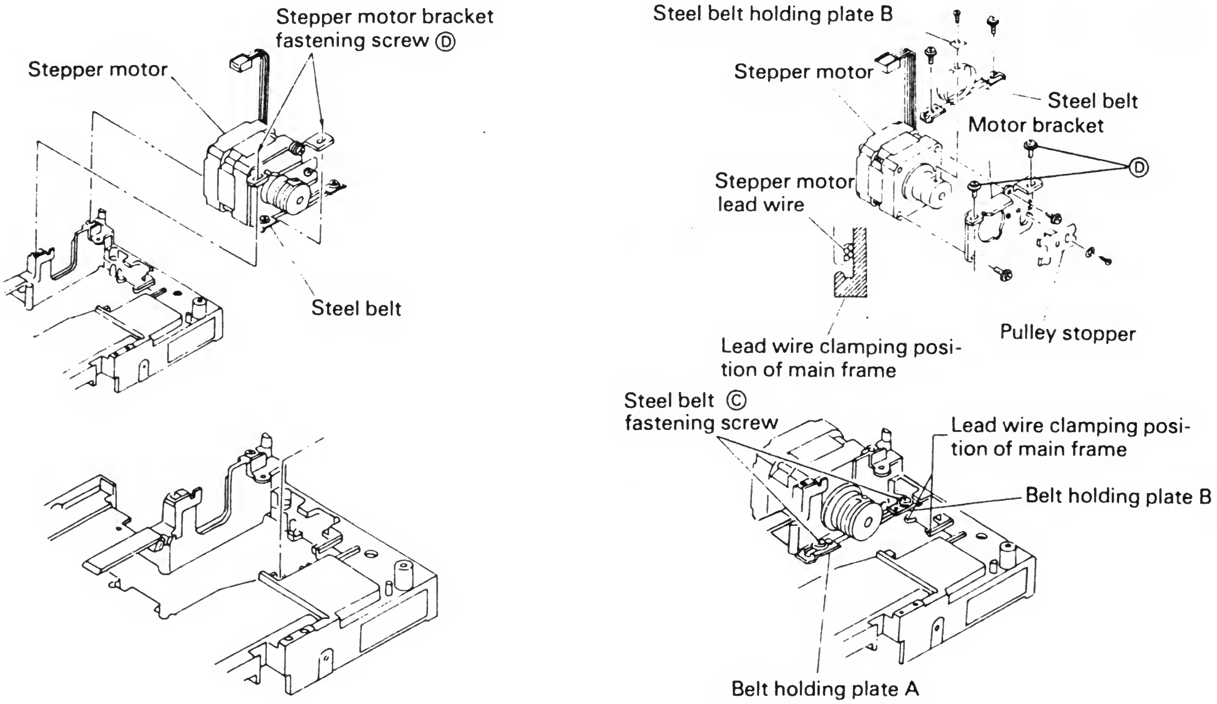

Stepper motor bracket fastening screw Ⓓ
Stepper motor
Steel belt
Steel belt holding plate B
Stepper motor
Steel belt
Motor bracket
Ⓓ
Stepper motor lead wire
Pulley stopper
Lead wire clamping position of main frame
Steel belt Ⓒ fastening screw
Lead wire clamping position of main frame
Belt holding plate B
Belt holding plate A

FIGURE 5-15. STEPPER MOTOR REMOVAL/REPLACEMENT

5.3.10 Stepper Motor Replacement (Figure 5-15)

1. Attach the motor brush and pulley stopper to the stepper motor. Secure the pulley stopper at the center of the attachement area and apply adhesive to the screw.

2. Position the steel belt on the stepper motor pully (Figure 5-15) and install the belt holding plate and the securing screws. Tighten the screws to a temporary torque of 2.0 Kg/cm.

3. Install the stepper motor on the frame and temporarily tighten the motor bracket securing screws to about 2.0 Kg/cm.

4. Secure the steel belt to the lower carriage and belt tension so that the divisions in the belt form parallel lines, then tighten the screws securing the belt holding plates A and B to approximately 2.0 - 6.0 Kg/cm.

5. Secure the stepper motor lead wires at the motor bracket and at the securing point on the frame, then connect the cable to the motor board.

6. Install the jacket lifter spring. (Section 5.3.8)

7. Install the subframe and front panel. (Section 5.3.6)

8. Install the main control board. (Section 5.3.4)

9. Adjust the off-track alignment.

5.3.11 Head Carriage Removal (Figure 5-16)

1. Remove the main control board. (Section 5.3.3)
2. Remove the front panel and subframe unit. (Section 5.3.5)
3. Remove the jacket lifter spring. (Section 5.3.7)
4. Disconnect the head lead wire from the clamp on the main frame.
5. Remove the screws which secure the steel belt to the carriage, and remove the belt from the carriage and from the belt tensioner.
6. Remove the sliding shaft securing plate, and remove the carriage at the steel belt side.
7. Remove the slide shaft and jacket lifter. Rotate the steel belt 90 degrees, and remove it together with the belt tension spring from the lower carriage.

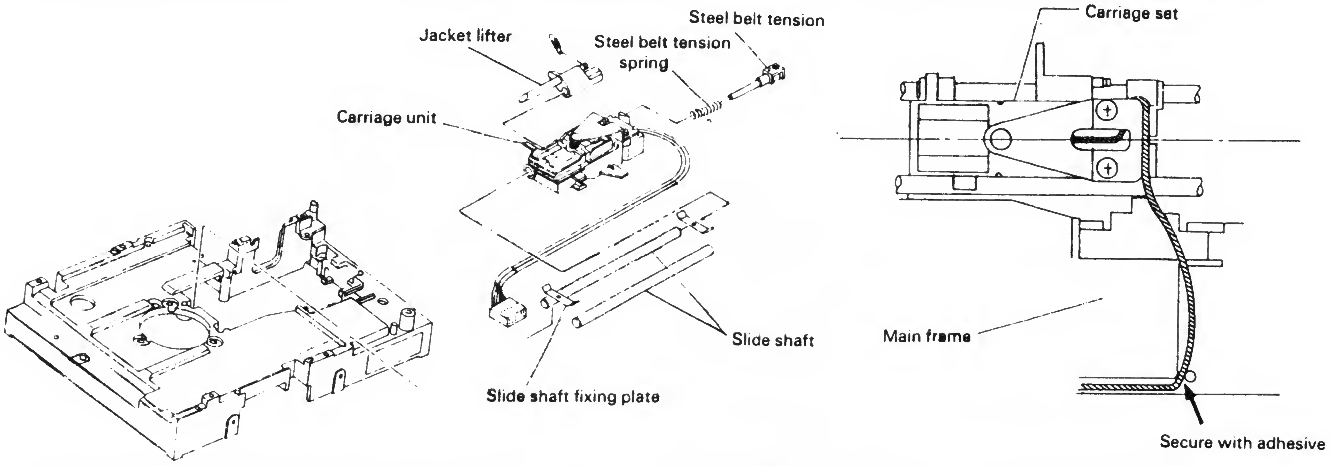


FIGURE 5-16. HEAD CARRIAGE REMOVAL/REPLACEMENT

5.3.12 Head Carriage Replacement (Figure 5-16)

1. Install the steel belt and the tension spring in the lower carriage.
2. Install the slide shaft and jacket lifter in the carriage, and install the carriage in the main frame by the slide shaft fixing plate.
3. Secure the head lead wire in the clamped position on the main frame and secure with adhesive. Check that the wires are positioned so that the head moves freely to all tracks.
4. Attach the jacket lifter spring. (Section 5.3.8)
5. Install the subframe unit and the front panel. (Section 5.3.6)
6. Install the main control board. (Section 5.3.4)
7. Adjust the off-track alignment, azimuth, index sensor position, and the track 00 sensor position.

5.3.13 Upper Carriage Removal (Figure 5-17)

1. Remove the main control board. (Section 5.3.3)
2. Remove the front panel and subframe unit. (Refer to Section 5.3.5)
3. Dissconnect the head lead wires from the main frame.
4. Remove the screws which secure the upper carriage, then remove the upper carriage holding plate and holding spring. Lift the upper carriage from the mechanism.
5. Disconnect the Side 1 lead wire from the connector, and raise the hook of the contact.

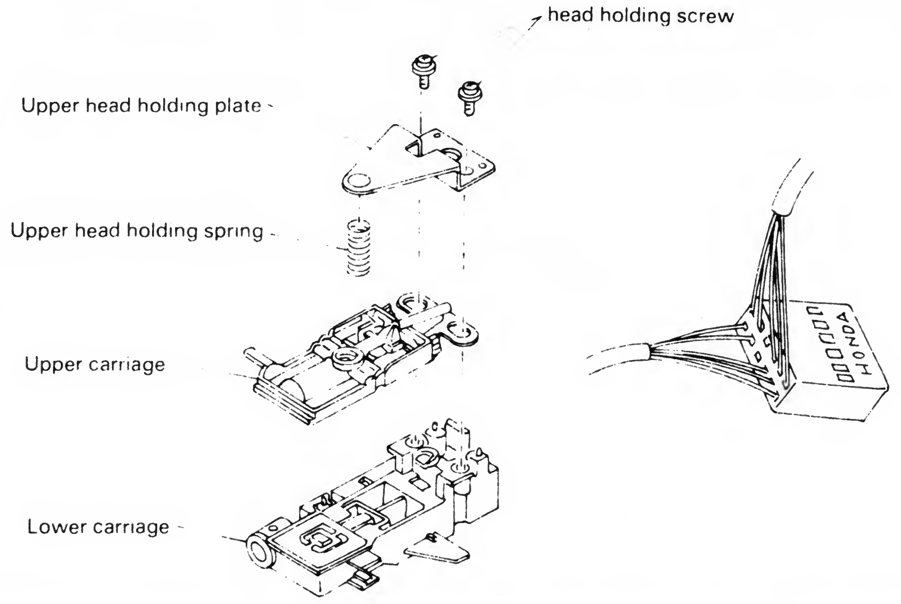


FIGURE 5-17. UPPER CARRIAGE REMOVAL/REPLACEMENT

5.3.14 Upper Carriage Replacement (Figure 5-17)

1. Position the upper carriage and install the upper carriage holding plate and holding spring. Securing them temporarily with the head holding screws.
2. Connect the Side 1 lead wire to the connector.
3. Secure the head lead wires with adhesive in the clamped position on the main frame. Check that the wires are positioned so that the head moves freely to all tracks.
4. Install the subframe and the front panel. (Section 5.3.6)
5. Adjust the off-track alignment index sensor position and the track 00 sensor position.
6. Install the main control board. (Section 5.3.4)

5.3.15 **Drive Motor Removal** (Figures 5-18 and 5-19)

1. Remove the main control board. (Section 5.3.3)
2. Remove the front panel and subframe. (Section 5.3.5)
3. Disconnect the level wires to the head solenoid, track 00 sensor, and stepper motor from the motor board.
4. Remove the motor securing screws and remove the motor unit.
5. Remove the magnet from the drive the motor board unit.
6. Remove the insulation sheet and pulley securing plate from the drive motor unit, then remove the pulley from the pulley securing plate.

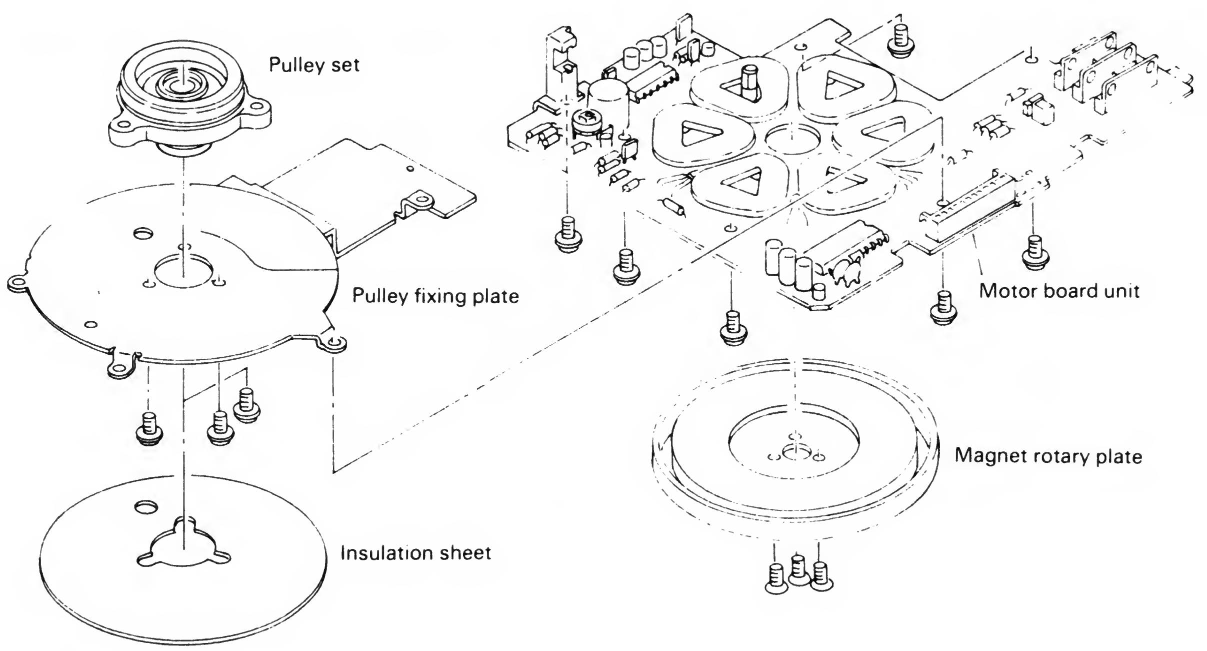


FIGURE 5-18. DRIVE MOTOR REMOVAL/REPLACEMENT (CONTINUED)

5.3.16 Drive Motor Replacement (Figures 5-18 and 5-19)

1. Install the pulley on the pulley securing plate.
2. Install the insulation sheet and pulley securing plate to the drive board unit.
3. Attach the magnet rotary plate to the drive motor board unit.
4. Install the spindle motor unit in the main frame, tightening the screws to 3.0 - 8.0 Kg/cm. Rotate the disk pulley to verify that it moves freely and evenly.
5. Connect the lead wires to the motor board.
6. Install the subframe and the SD-521 front panel. (Section 5.3.6)
7. Install the main control board. (Section 5.3.4)

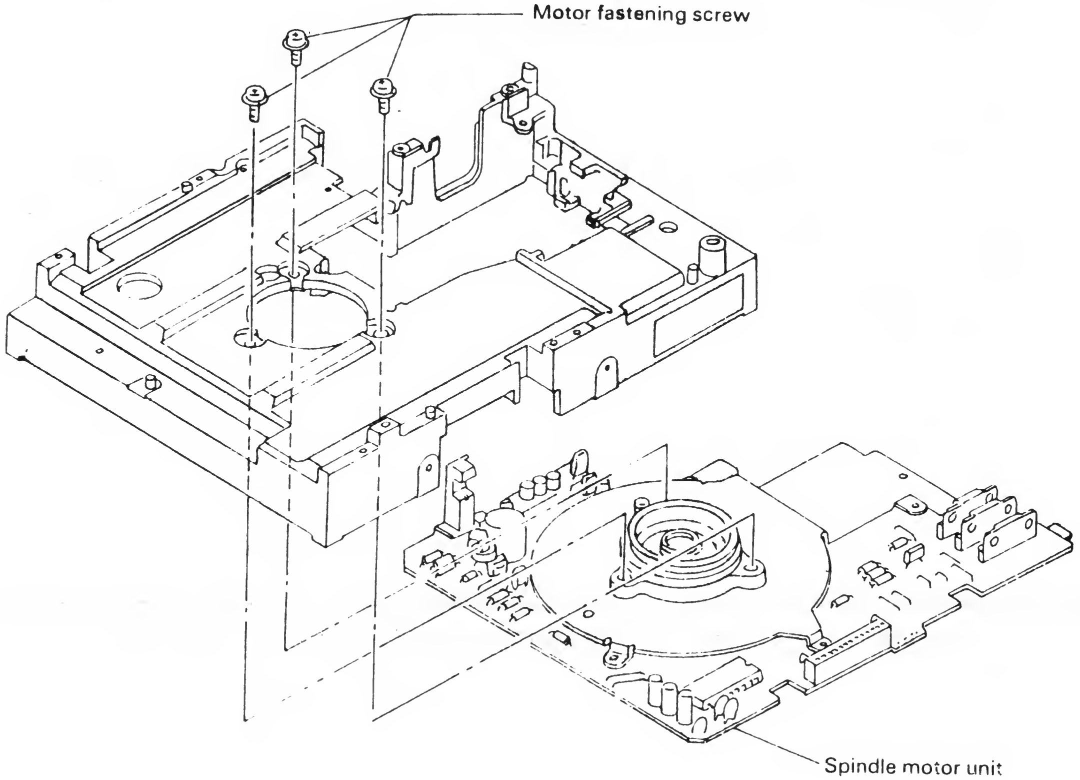


FIGURE 5-19. DRIVE MOTOR REMOVAL/REPLACEMENT

5.4 KEYBOARD DISASSEMBLY AND ASSEMBLY

5.4.1 Keyboard Case Removal (Figure 5-20)

1. Disconnect the keyboard cable from the main unit and the keyboard.
2. Turn the keyboard upside down and remove screws (A) from the lower case. Lift the case straight up to remove.

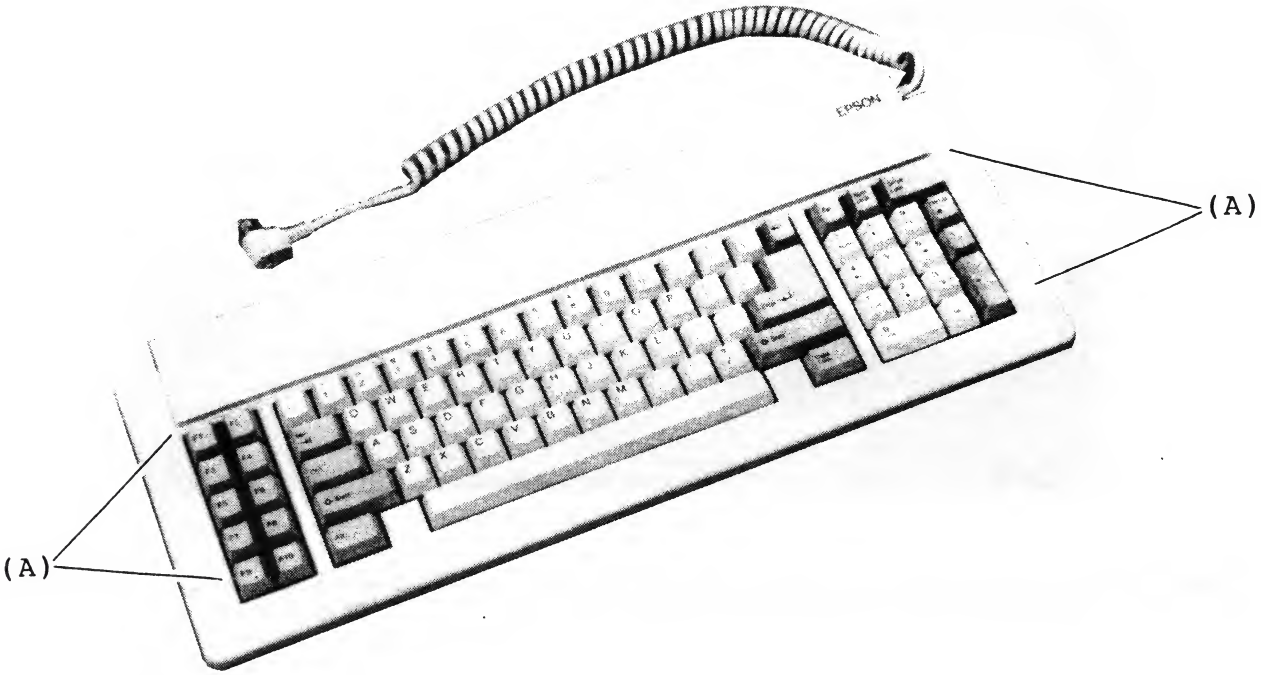


FIGURE 5-20. KEYBOARD CASE REMOVAL/REPLACEMENT

5.4.2 Keyboard Case Replacement (Figure 5-20)

1. Install the keyboard case with screws (A) and install the keyboard cable.

5.4.3 Keyboard Ciruit Board Removal (Figure 5-21)

1. Remove the keyboard case. (Section 5.4.1)
2. Remove four screws (A) and the accompanying brackets.
3. Remove 11 screws from the circuit board and carefully remove the board.

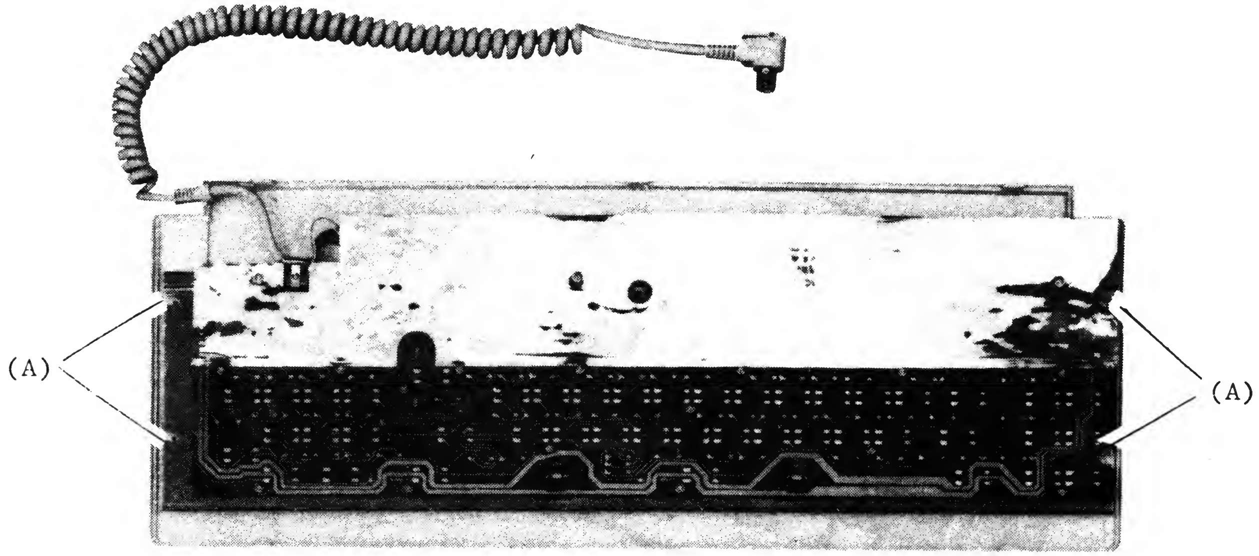


FIGURE 5-21. KEYBOARD CIRCUIT BOARD REMOVAL/REPLACEMENT

5.4.4 Keyboard Circuit Board Replacement (Figure 5-21)

1. Install the circuit with 11 screws.
2. Install the keyboard case. (Section 5.4.2)

5.5 HD-860 DISASSEMBLY AND ASSEMBLY

5.5.1 Main PCB Removal

(1) Remove two M3 mounting screws securing the front bezel from the mounting frame to detach the front bezel. (Figure 5-22)

CAUTION

LED is connected to the PCB via the lead wires, so be careful not to damage it when you remove the front bezel.

(2) Remove LED from the front bezel by slightly pushing the hook of the front bezel.

(3) Disconnect the sub track zero sensor cable and the head cable.

CAUTION

These cables are flexible printed circuits and very easy to get damaged. Do not handle them roughly.

(4) Remove two M3 mounting screws of the radiator of the spindle motor driver IC from the HDA. (Figure 5-23)

(5) Remove five M2.5 mounting screws securing the PCB from the mounting struts (Figure 5-23)

(6) Disconnect the spindle motor cable (white connector) shown in Figure 5-24. Pull it upwardly. Be careful not to damage other cables.

(7) Disconnect the carriage lock cable (blue connector), the main track zero sensor cable (red connector) and the stepper cable (black connector) in this order. Refer to Figure 5-24 for the location of each cable.

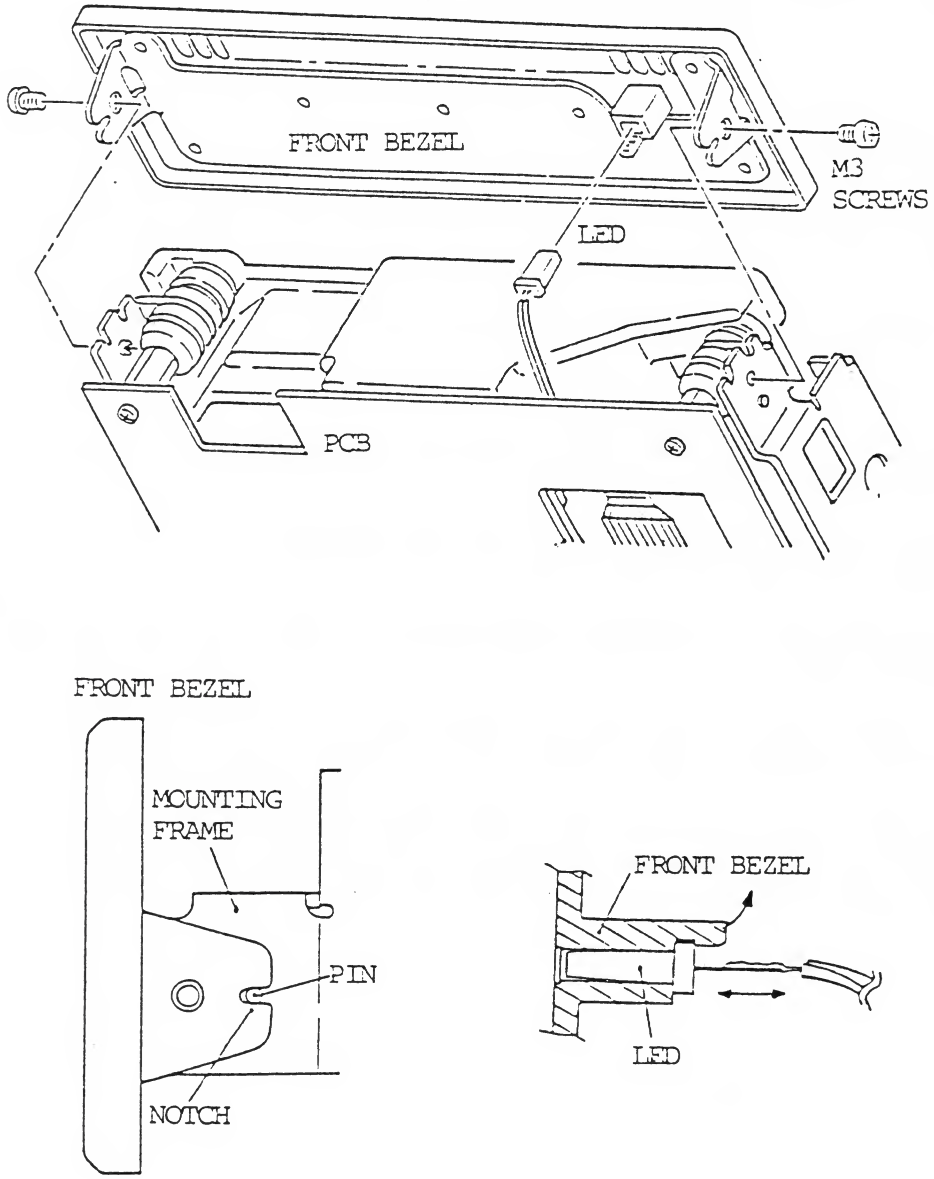


FIGURE 5-22. FRONT BEZEL REMOVAL/REPLACEMENT

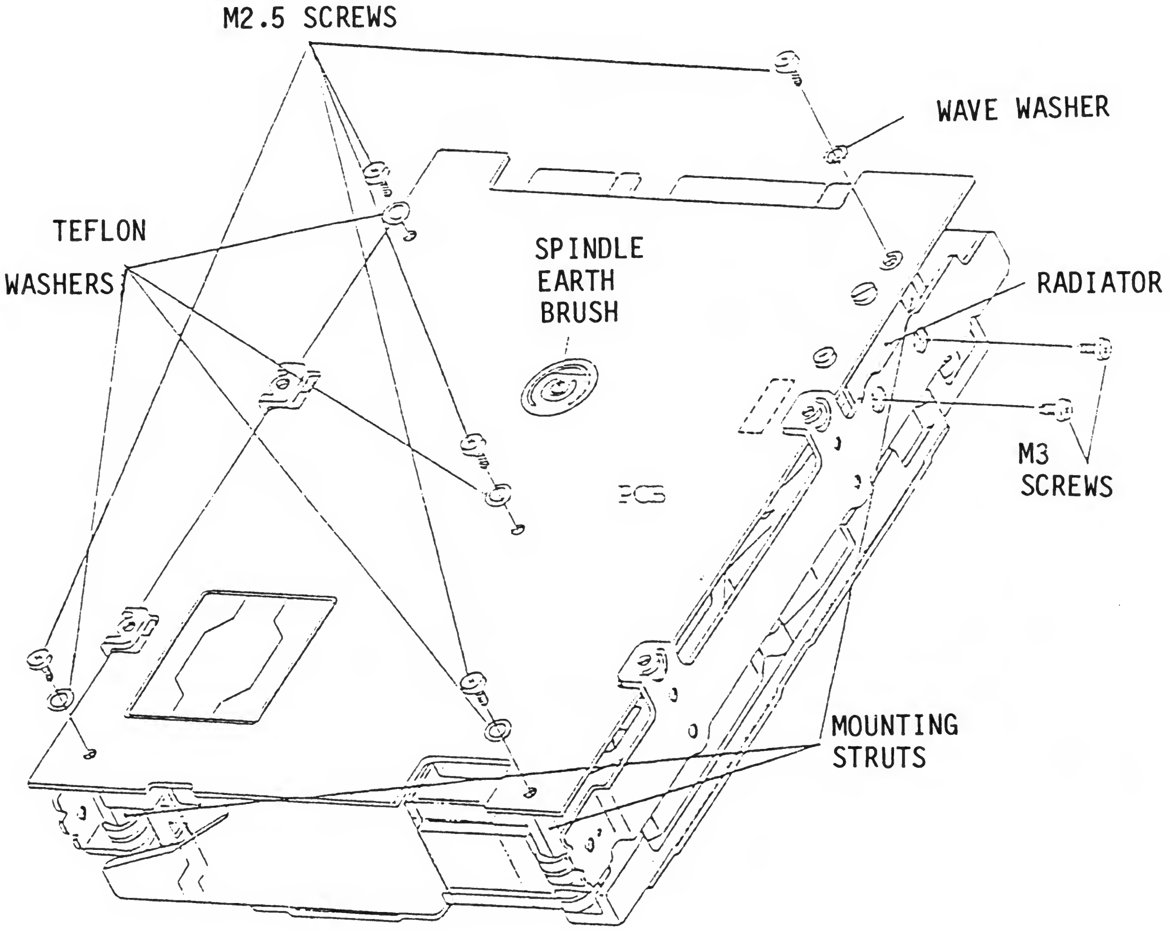


FIGURE 5-23. REMOVE PCB

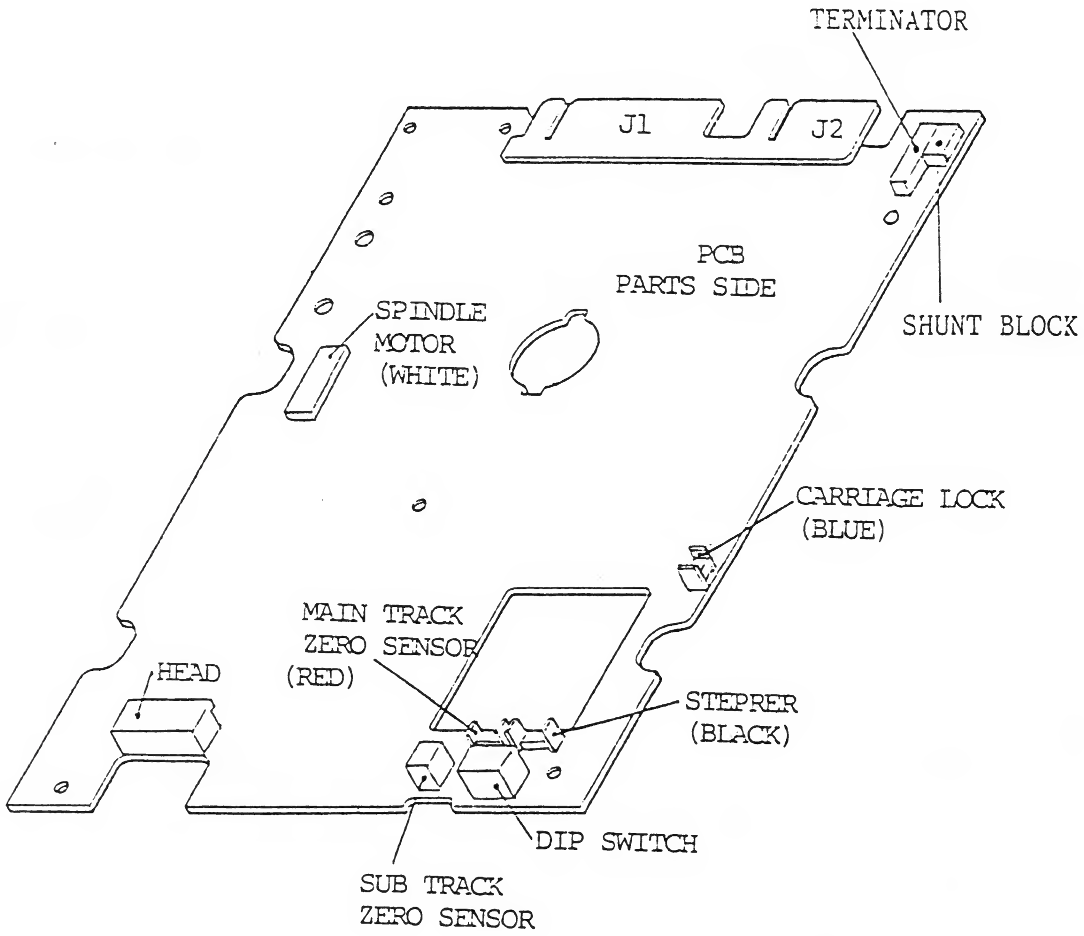


FIGURE 5-24. CONNECTORS LOCATION

5.5.2 Main PCB Replacement

(1) Connect the carriage lock cable (blue), the main track zero sensor cable (red) and the stepper cable (black) to the PCB in this order.

(2) Connect the spindle motor cable (white). Insert it with adjusting the position of both the motor connector and the PCB connector.

(3) Secure the PCB to mounting struts with five M2.5 mounting screws. Locking torque is 2Kg-cm or 1.8 pound-inch. Make sure that the center of the spindle earth brush in the PCB touches the top of the spindle motor shaft. (Figure 5-23)

(4) Secure the radiator of spindle motor driver IC to the HDA with two M3 mounting screws. Locking torque is 3 Kg-cm or 2.7 pound-inch. Make sure that the radiator is secured tightly to the HDA without space.

(5) Connect the sub track zero sensor cable and the head cable to the PCB.

(6) Hang the LED on the hook of the front bezel. (Figure 5-22)

(7) Secure the front bezel to the mounting frame with two M3 mounting screws. Locking torque is 5 Kg-cm or 4.4 pound-inch. Position the pins near screw holes of mounting frame in the notches of the front bezel. (Figure 5-22)

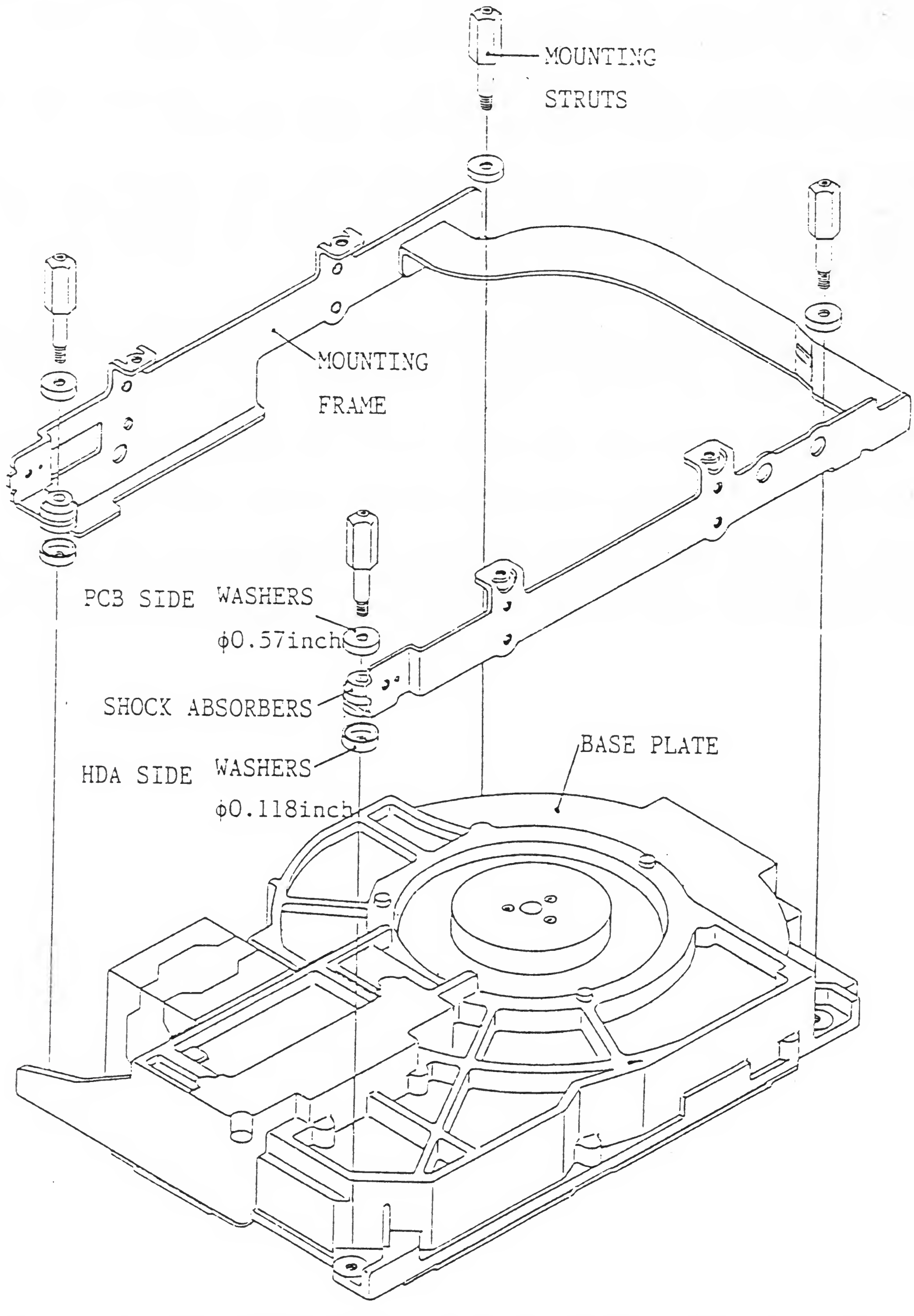


FIGURE 5-25. REMOVE MOUNTING FRAME

5.5.3 Main Track Zero Sensor Removal

(1) Remove a M2.5 mounting screw of the ground cable from the mounting frame.

(2) Remove four mounting struts from the mounting frame. Washers of shock absorbers can be also detached. There are four washers at the PCB side and two washers at the HDA side. The washer of each side has different diameter from the other side one. Remember that the diameter of the HDA side washer is Ø0.118 inch or Ø3 mm and that of the PCB side washer is Ø0.157 inch or Ø4 mm. (Figure 5-25)

(3) Remove the mounting frame from the HDA. (Figure 5-25)

(4) Before removing the main track zero sensor, mark the sensor position with the marking tape so that the new sensor can be easily adjusted. Be careful that the marking error must be within 0.004 inch or 1 mm.

(5) Remove two M2 mounting screws from the stepper. (Figure 5-26)

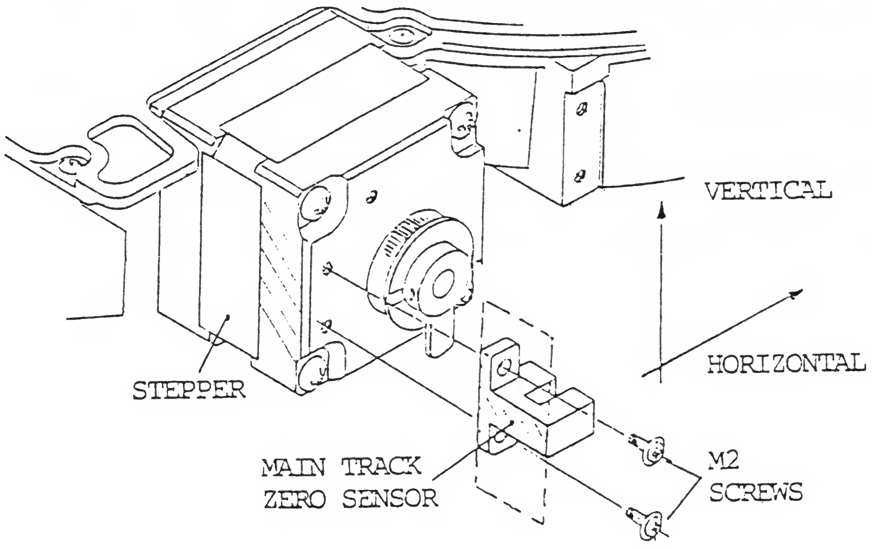


FIGURE 5-26. REMOVE TRACK ZERO SENSOR

Temporary Installation

Before the sensor is secured tightly, it must be installed temporarily and adjusted.

(1) Secure the main track zero sensor with two M2 mounting screws as shown in Figure 5-26. Adjust the sensor in reference to the marking tape in the vertical direction. In horizontal direction, adjust the sensor so that the shaded portions of the stepper and the sensor side of the main track zero sensor PCB in Figure 5-26 are on the same plane. Locking torque is 1 Kg-cm or 0.9 pound-inch.

(2) Secure mounting struts to the HDA with locking torque of less than 5 Kg-cm or 4.4 pound-inch.

(3) Connect cables of the carriage lock (blue), the main track zero sensor (red) and the stepper (black) to the PCB in this order. (Figure 5-24)

(4) Connect the spindle motor cable (white) to the PCB.

(5) Secure the PCB to the mounting struts with five M2.5 mounting screws. Locking torque is less than 2 Kg-cm or 1.8 pound-inch. (Figure 5-23)

(6) Secure the radiator to the HDA with two M3 mounting screws. Locking torque is less than 3 Kg-cm or 2.7 pound-inch. (Figure 5-23)

(7) Connect the cable of the sub track zero sensor to the PCB.

(8) Connect the power cable, but don't power on.

5.5.4 Main Track Zero Sensor Replacement

Before installing the main track zero sensor, you must remove the PCB first again.

(1) Disconnect the power cable from the PCB.

(2) Disconnect the sub track zero sensor cable from the PCB.

(3) Remove two mounting screws of radiator from the HDA. (Figure 5-23)

(4) Disconnect the spindle motor cable from the PCB. (Figure 5-24)

(5) Disconnect cables of the carriage lock (blue), the main track zero sensor (red) and the stepper (black) in this order. (Figure 5-25)

(6) Remove four mounting struts.

(7) Remove the marking tape.

(8) Secure the mounting frame to the HDA with four mounting struts and shock absorbers. Make sure that washers for shock absorbers are in the correct direction (see step 2 in "Temporary Installation") and the cable of the carriage lock is in-side of the mounting frame. Locking torque is 5 Kg-cm or 4.4 pound-inch.

(9) Install the PCB by performing steps 1 through 7 in 5.5.2.

5.5.5 Carriage Lock Removal

Remove one M2 stepped mounting screw and two M2.5 assembling screws in this order. (Figure 5-27)

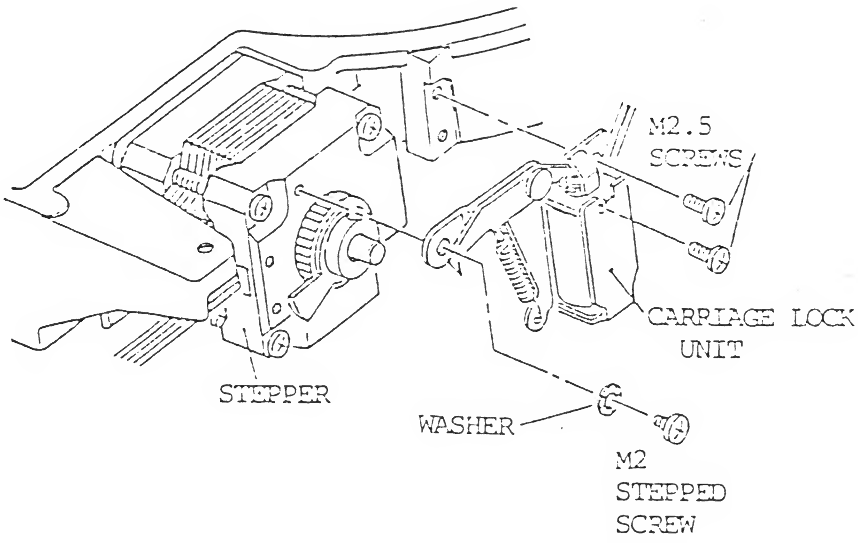


FIGURE 5-27. REMOVE CARRIAGE LOCK

5.5.6 Carriage Lock Replacement

CAUTION

Be careful not to damage the gear wheel with the carriage lock pawl.

(1) Secure carriage lock unit with one stepped mounting screw and two M2.5 assembling screws temporarily. Don't forget to insert a wave washer. (Figure 5-27)

(2) Make sure that the carriage lock unit can be moved to adjust easily by hand.

5.6 SD-581L DISASSEMBLY AND ASSEMBLY

Be sure to turn off the power before disassembly and assembly. Then remove the power connector (J1) and the signal connector (J2). If the disk is in the disk drive, remove it and keep it in a safe place.

The following is the flow chart of the SD-581L The disassembly and assembly is to be done by this procedure :

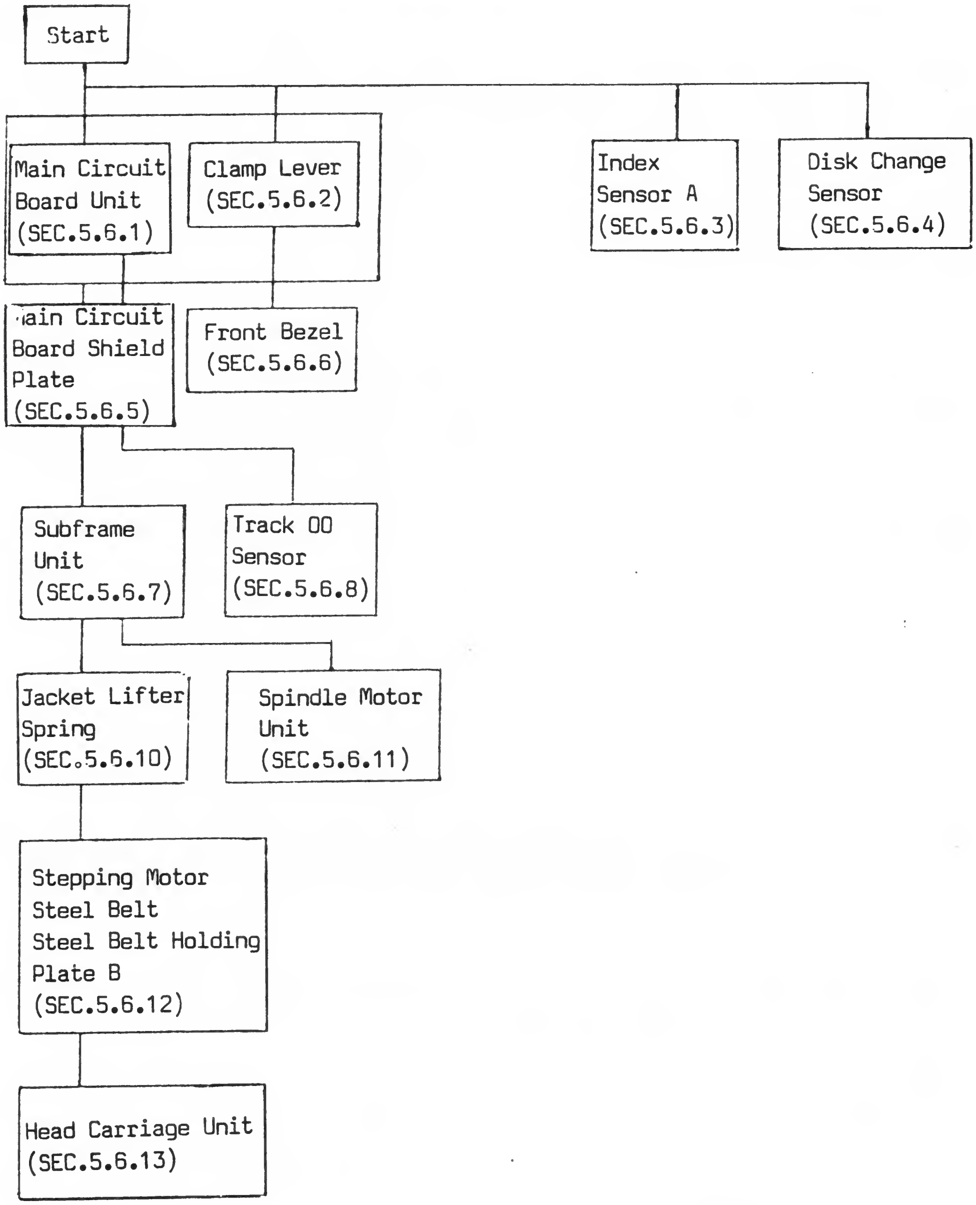

Start
Main Circuit Board Unit (SEC.5.6.1)
Clamp Lever (SEC.5.6.2)
Index Sensor A (SEC.5.6.3)
Disk Change Sensor (SEC.5.6.4)
Main Circuit Board Shield Plate (SEC.5.6.5)
Front Bezel (SEC.5.6.6)
Subframe Unit (SEC.5.6.7)
Track 00 Sensor (SEC.5.6.8)
Jacket Lifter Spring (SEC.5.6.10)
Spindle Motor Unit (SEC.5.6.11)
Stepping Motor Steel Belt Steel Belt Holding Plate B (SEC.5.6.12)
Head Carriage Unit (SEC.5.6.13)

FIGURE 5-28. DISASSEMBLY FLOW CHART

5.6.1 Main Circuit Board

Disassembly

1) Pull up the head lead wire clamper to raise the head lead wire a little. (Four places)
   Note : ● As the head lead wire clamper can break easily, do not flex it many times.
2) Remove the index sensor A connector (J4-P4) and disk change sensor connector (J6-P6).
3) Remove the main circuit board setscrews (a), (b), (c) and (d) and the washer (e).
   CS M2.5 x 4·········a
   CS M2.5 X 6·········b
   CS M2.5 x 6·········c
   CP M2.5 x 5·········d
   OW ϕ 2.6 ·········e
4) Raise the main circuit board in parallel with the main frame and remove the interboard connector (J3-P3).
   Note : ● Lift the connector by both the ends for removal.
5) Remove the head lead wire connector (J5-P5).

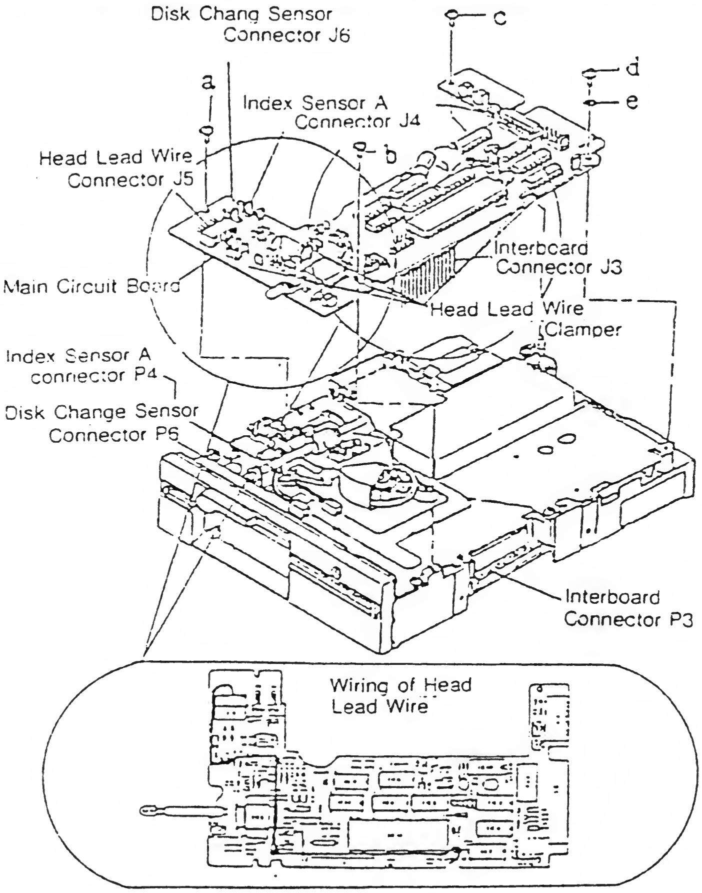


FIGURE 5-29. MAIN CIRCUIT BOARD DISASSEMBLY AND ASSEMBLY

Assembly

1) Adjust the pins of the connector (J3) on the main circuit board properly to the motor-side connector (P3) and insert them straight.
   Note : ● In inserting the connector, push the main-circuit -board-side connector by both its ends and the motor circuit board at the same time.
2) Connect each of the connectors of the head lead wire, the index sensor lead wire and the disk change sensor lead wire.
3) Secure the main circuit board with the setscrews (a), (b), (c) and (d) and the washer (e). (Screw tightening torque : about 6.0 kg. cm)
4) Fasten the head lead wire by bending the head lead wire clamper.

5.6.2 Clamp Lever

Disassembly

1) Put the clamp lever in the eject position and remove the clamp lever setscrew (a) by the hexagonal wrench (M3).
   Hexagon socket head cone- pointed setscrew M2.5 × 3·········a
2) Pull out the clamp lever from the lever shaft and the hole of the front bezel.

Assembly

1) Fit the clamp lever on the lever shaft by inserting it through the hole of the front bezel.
   Note : ● Set the upper surface of the lever in parallel with the bezel.
2) Secure the clamp lever setscrew (a) with the hexagonal wrench.
   (Screw tightening torgue : about 3.0 kg. cm)

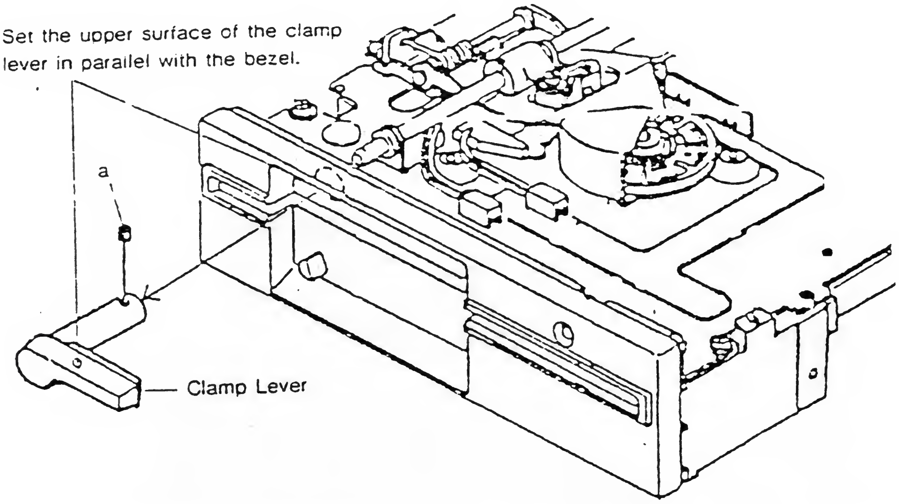

Set the upper surface of the clamp lever in parallel with the bezel.
a
Clamp Lever

FIGURE 5-30. CLAMP LEVER

5.6.3 Index Sensor A

Disassembly

1) Remove the index sensor A setscrew (a) and dismount the index sensor A.

CPSP M2.5 × 11 ·········a

Assembly

1) Mount the index sensor A on the subframe unit by tightening the index sensor A setscrew (a) provisionally.
(Provisional tightening torque : 1.5 kg. cm)
2) Adjust the index position.

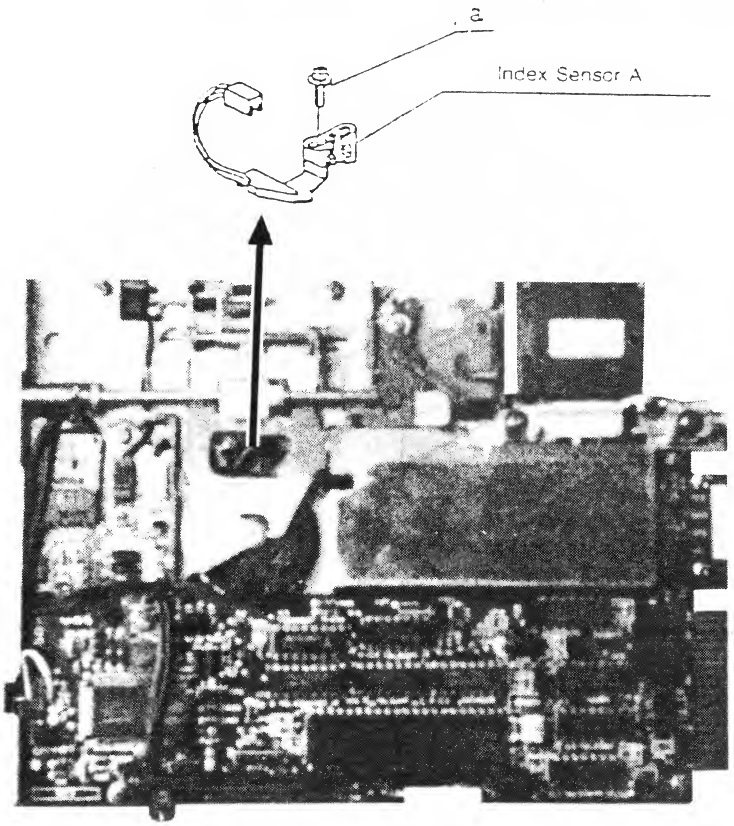


FIGURE 5-31. INDEX SENSOR A

5.6.4 Disk Change Sensor

Disassembly

1) Remove the disk change sensor lead wire connector J6-P6.
2) Remove the disk change sensor setscrew (a).
   CS (precision screw) M1.6 × 5.5 ·········a
3) Dismount the disk change sensor from the subframe.
4) Pass the disk change sensor lead wire connector P6 under the lever shaft.
5) Remove the lead wire by passing it under the disk change sensor contact point of the collet lever and the collet lever spring.

Assembly

1) Pass the disk change sensor lead wire connector P6 under the collet lever spring, the disk change sensor contact point of the collet lever and the lever shaft.
2) Connect the disk change sensor lead wire connectors P6 and J6 with each other.
3) Set the disk change sensor on the subframe and tighten the setscrew (a).
   (Screw tightening torque : about 2.0 kg. cm)

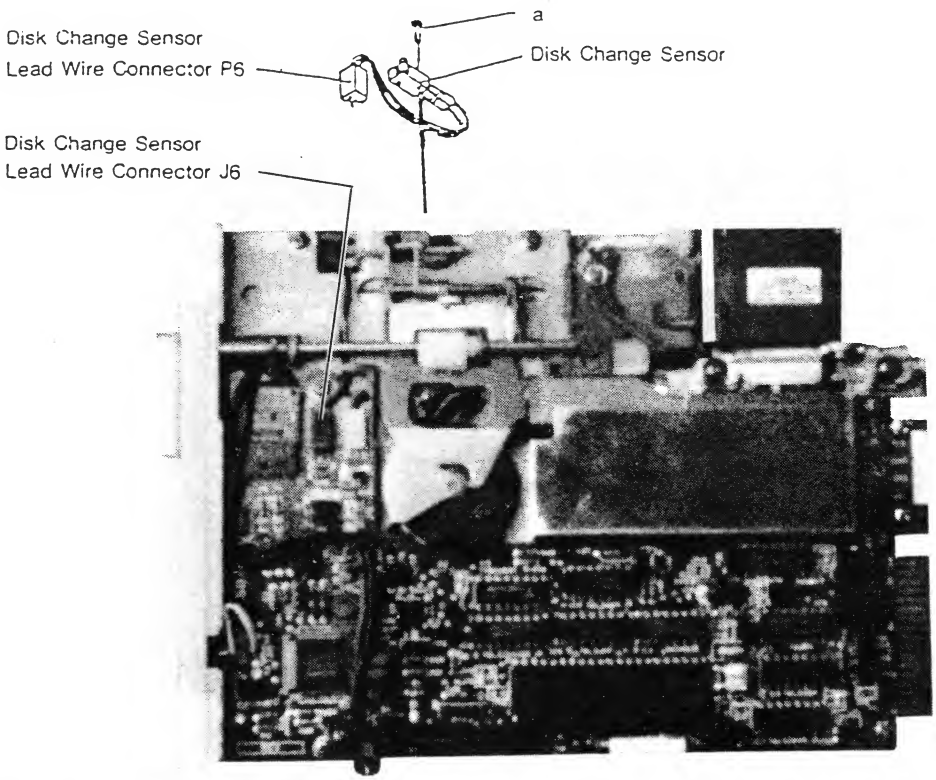

a
Disk Change Sensor
Disk Change Sensor Lead Wire Connector P6
Disk Change Sensor Lead Wire Connector J6

FIGURE 5-32. DISK CHANGE SENSOR

5.6.5 Main Circuit Board Shield Plate

Disassembly

1) Dismount the main circuit board unit.
2) Remove the setscrew (a) securing the main circuit board shield plate and dismount the main circuit board shield plate from the subframe.

   Taptight CS M2 × 4 ·········a

Assembly

1) Set the main circuit board shield plate and tighten the setscrew (a).
   (Screw tightening torque : about 4.5 kg.cm.)
2) Mount the main circuit board unit.

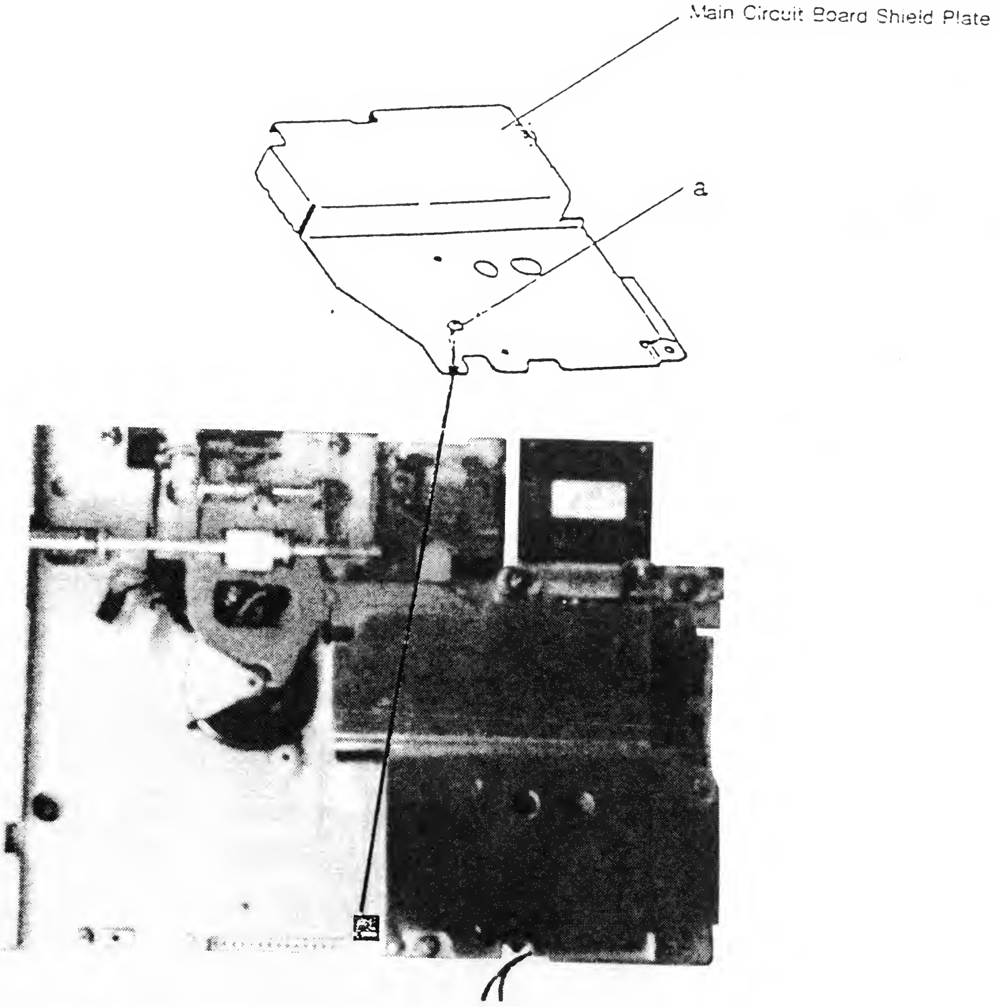


FIGURE 5-33. MAIN CIRCUIT BOARD SHIELD PLATE

5.6.6 Front Bezel

Disassembly

1) Remove the clamp lever.
2) Remove the front bezel setscrews (a) and (b) and take off the front bezel toward you.

CPSP M2.5 × 6 ·········a, b

Assembly

1) Set the front bezel, and fix it with the setscrews (a) and (b), pressing the front bezel against the frame.
   (Screw tightening torque : about 4.5 kg.cm.)
2) Attach the clamp lever.

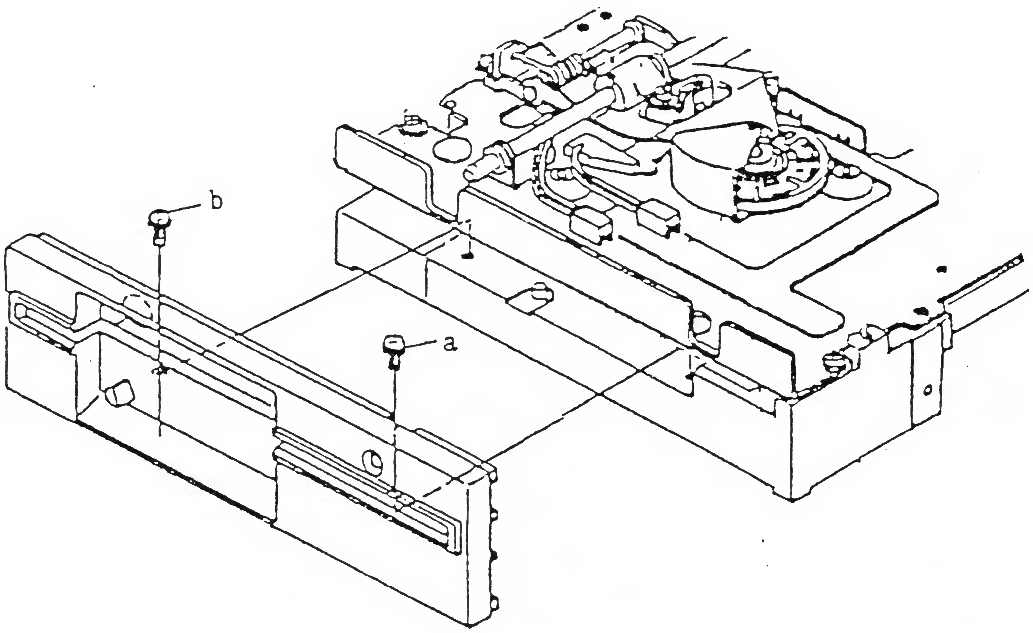


FIGURE 5-34. FRONT BEZEL

5.6.7 Subframe Unit

Disassembly

1) Dismount the main circuit board.
2) Take off the clamp lever.
3) Dismount the main circuit board shield plate.
4) Remove the subframe unit setscrews (a) to (d).

   CS M2.5 × 6 ········ a, b, c, d

5) Dismount the subframe unit from the main frame.

   Note : ● Be sure to perform the removal of the subframe with a clean paper or clean, lint-free paper inserted between the upper and lower heads. This is to prevent the upper and the lower head from sticking together.

6) Remove the head load lever.

Assembly

1) Attach the head load lever to the subframe unit.
2) Adjust the subframe unit to the positioning pin on the main frame, push it against the right side (the LED side of the front bezel) while pulling it toward you, and secure it with the setscrews (a) to (d)

   (Screw tightening torque : about 4.0 kg. cm)

   Notes : ● Have the edge of the write protect sensor on the spindle motor circuit board engage with the slit in the subframe.
   ● Place the arm of the upper carriage on the collet lever.

3) Remove the clean paper from between the upper and lower heads.
4) Attach the main circuit board shield plate.
5) Attach the clamp lever.
6) Mount the main circuit board unit.
7) Adjust the index position and the head load lever gap.

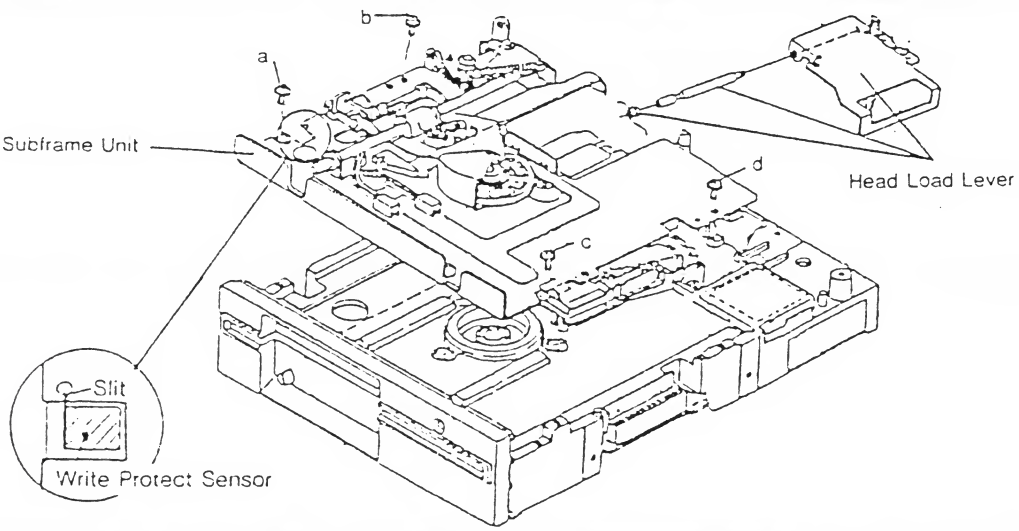


FIGURE 5-35. SUBFRAME UNIT ASSEMBLY

5.6.8 Track 00 Sensor

Disassembly

1) Dismount the main circuit board unit.
2) Remove the main circuit board shield plate.
3) Remove the track 00 sensor connector P6 from the connector J6 on the motor circuit board.
4) Take off the track 00 sensor adjusting screw (a), and slide the track 00 sensor in the horizontal direction and then pull it out upwards.

CPSP (Polished round) M2.5 × 6 ·········a

Assembly

1) Set the track 00 sensor on the main frame and tighten the adjusting screw (a) provisionally.

(Provisional tightening torque : 1.5 kg.cm)

2) Connect the track 00 sensor connector P6 to the connector J6 on the motor circuit board.
3) Attach the main circuit board shield plate.
4) Mount the main circuit board unit.
5) Adjust the position of the track 00 sensor.

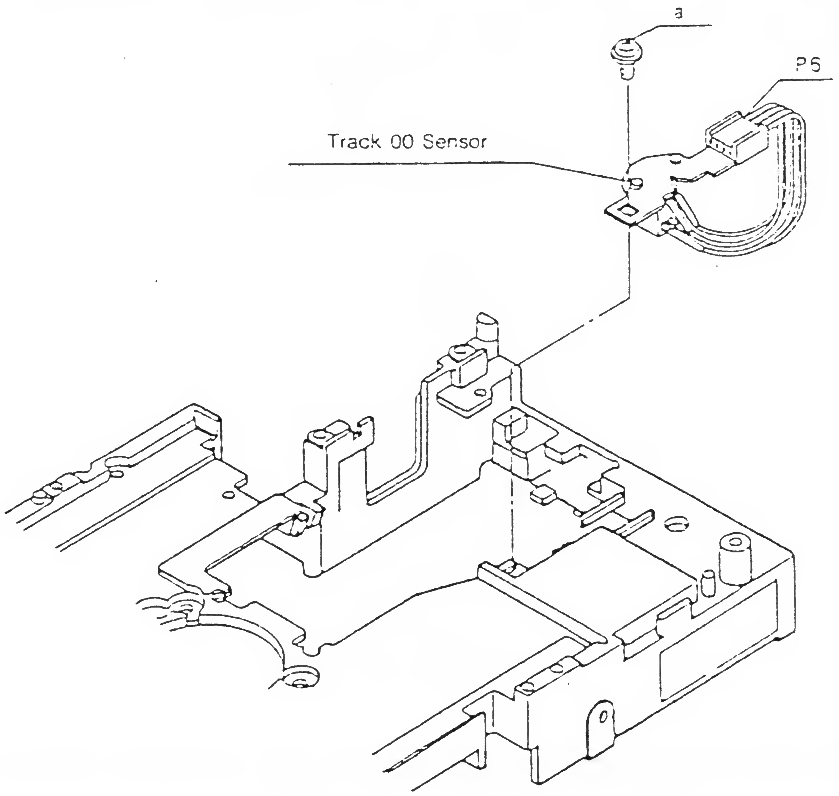


FIGURE 5-36. TRACK 00 SENSOR

5.6.9 Head Load Lever

Disassembly

1) Dismount the main circuit board unit.
2) Remove the main circuit board shield plate.
3) Remove the retaining ring RE (a) and the head load lever spring from the head load lever fulcrum shaft and then pull out the head load lever fulcrum shaft.
   RE 2.3 ·········a
4) Push down the collet lever while lifting the upper carriage so that the C part of the head load lever passes between the upper carriage arm and the collet lever and comes to the position above the arm of the upper carriage.
5) Move the head load lever in the carriage direction, and pull out the head load lever, passing the head load roller through the gap between the subframe and the stepping motor.

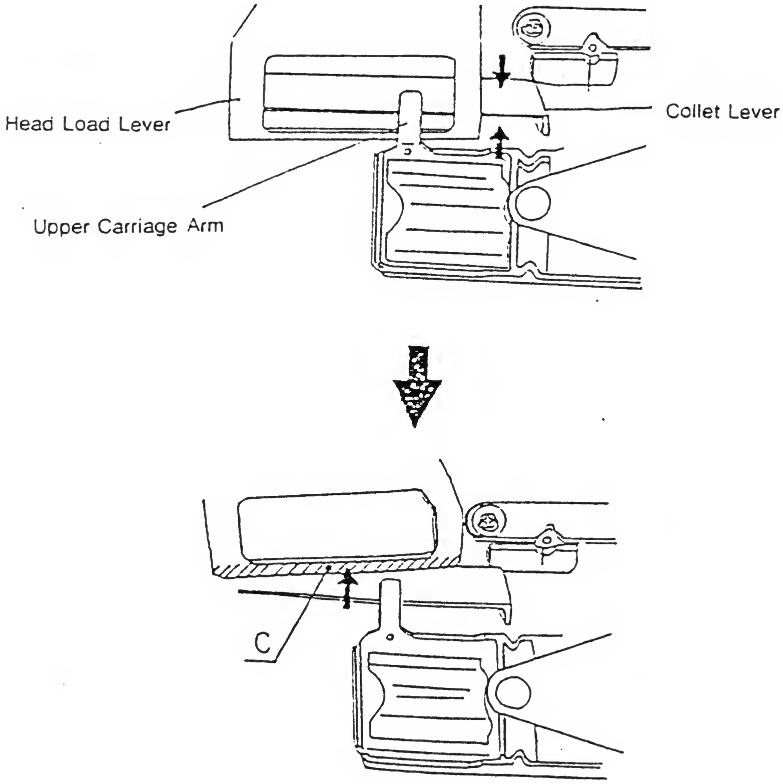


FIGURE 5-37. HEAD LOAD LEVER

Assembly

1) Move the head load lever outward, passing the head load roller through the gap between the subframe and the stepping motor.
2) Push down the collet lever while lifting the upper head, so that the collet lever passes between the head load lever and the upper carriage arm and comes under the upper carriage arm.
3) Run the head load lever fulcrum shaft through the subframe and the head load lever, and lock it with the retaining ring RE (a). Run the head load lever spring through the fulcrum shaft and hook the spring to the head load lever and the subframe.
4) Perform necessary lubrication at the replacement or cleaning of the head load lever or the head load lever shaft.
5) Attach the main circuit board shield plate.
6) Mount the main circuit board unit.
7) Adjust the head load lever gap.

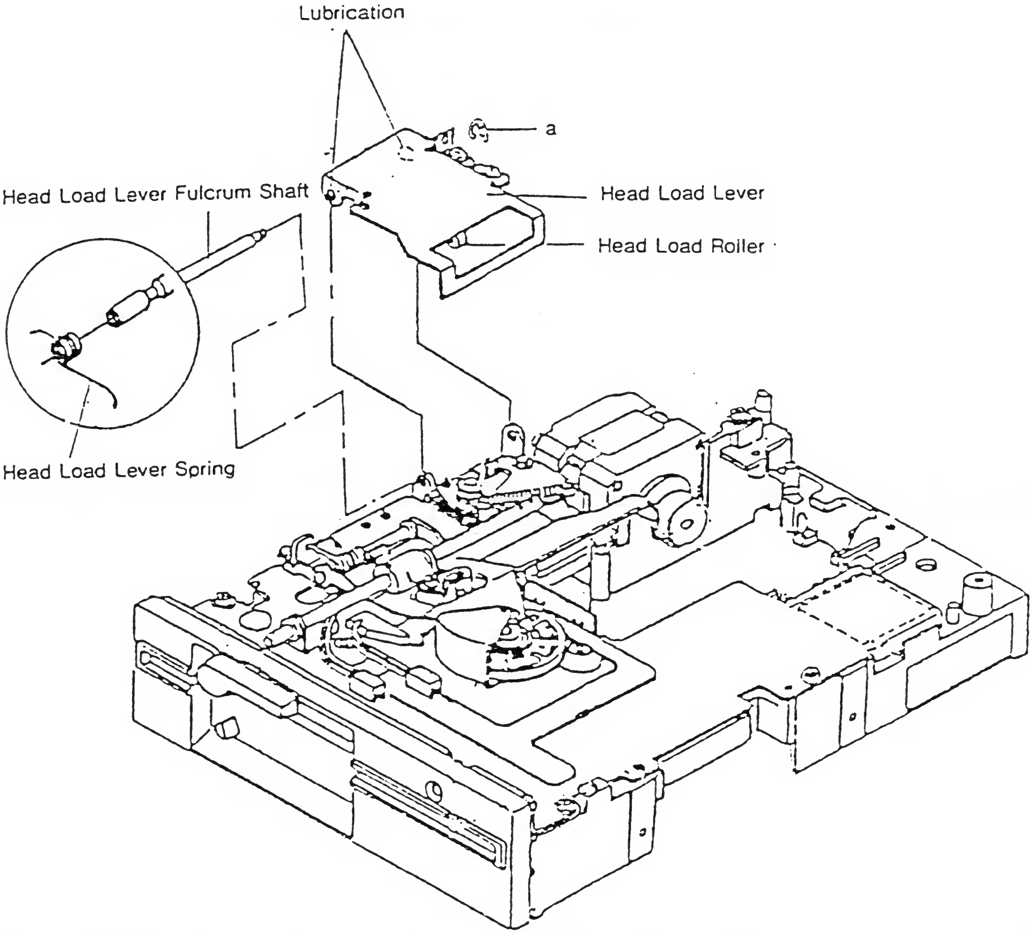


FIGURE 5-38. HEAD LOAD LEVER LUBRICATION DIAGRAM

5.6.10 Jacket Lifter Spring

Disassembly

1) Dismount the main circuit board unit.
2) Remove the main circuit board shield plate.
3) Remove the jacket lifter spring from the main frame and carriage.

Assembly

1) Move the carriage unit to the outermost position, and set the spring to the carriage and the main frame.
2) Hook up the jacket lifter spring with the main frame.
3) Attach the main circuit board shield plate.
4) Mount the main circuit board unit.

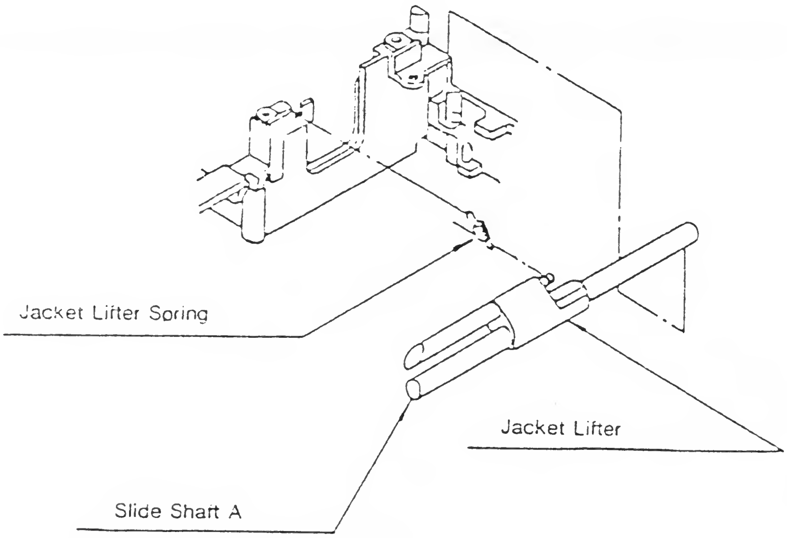


FIGURE 5-39. JACKET LIFTER SPRING

5.6.11 Spindle Motor Unit

Disassembly

1) Dismount the main circuit board unit.
2) Take off the clamp lever.
3) Remove the main circuit board shield plate.
4) Dismount the subframe unit.
5) Disconnect the lead wire connectors J9-P9, J6-P6 and J8-P8 of the head load solenoid, the track 00 sensor and the stepping motor which are all connected to the motor circuit board.
6) Remove the spindle motor setscrews (a), (b) and (c) and dismount the spindle motor unit.

CS M3 × 6 ·········a, b, c

Note : ● Be careful not to cause any scratch or damage to the spindle.

Assembly

1) Fix the spindle motor unit on the main frame with the setscrews (a), (b) and (c).
   (Screw tightening torque : about 6.0 kg.cm)
2) Connect the lead wire connectors J9-P9, J6-P6 and J8-P8.
3) Mount the subframe unit.
4) Attach the main circuit board shield plate.
5) Attach the clamp lever.
6) Mount the main circuit board.
7) Adjust the off-track and index positions.

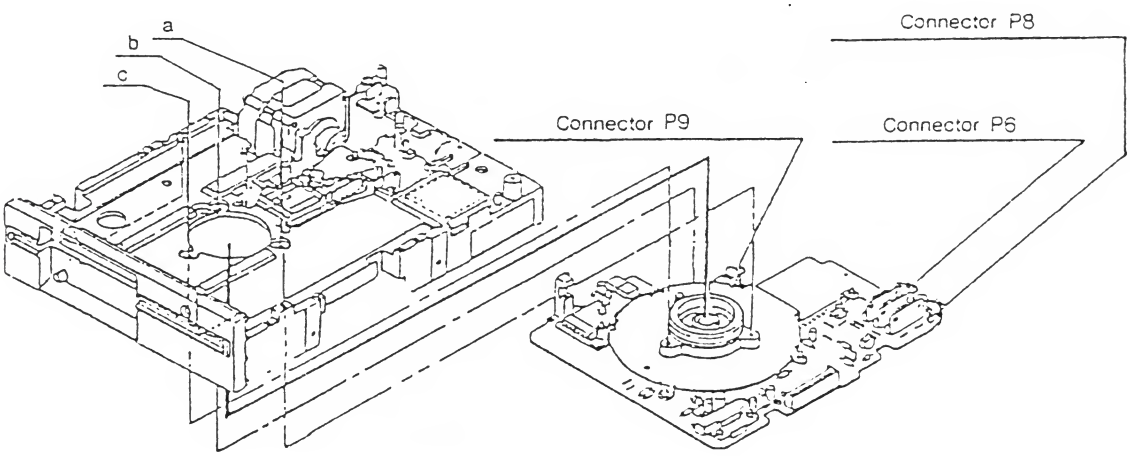


FIGURE 5-40. SPINDLE MOTOR UNIT

5.6.12 Stepping Motor Unit

Disassembly

1) Dismount the main circuit board unit.
2) Take off the clamp lever.
3) Remove the main circuit board shield plate.
4) Dismount the subframe unit.
5) Disconnect the stepping motor lead wire connector P8 from the motor circuit board connector J8.
6) Remove the jacket lifter spring.
7) Take off the steel belt setscrews (a) and (b) from the lower carriage.

   CPSP (polished round) M2.5 × 6 ·········a, b

   Note : ● Watch out for the tilting that can be caused at the pushing of the steel belt tensioner.
8) Disengage the steel belt from the steel belt tensioner by pushing the steel belt tensioner towards the lower carriage.
9) Remove the stepping motor bracket setscrews (c) and (d), and pull out the stepping motor upwards, taling care not to damage the steel belt.

   CPSP (polished round) M2.5 × 6 ·········c, d
10) Remove the steel belt holding plate B setscrew (e), using a phillips screwdriver for precision machine use, and remove the steel belt holding plate B and the steel belt.

    CP (precision screw) M2 × 4 ·········e

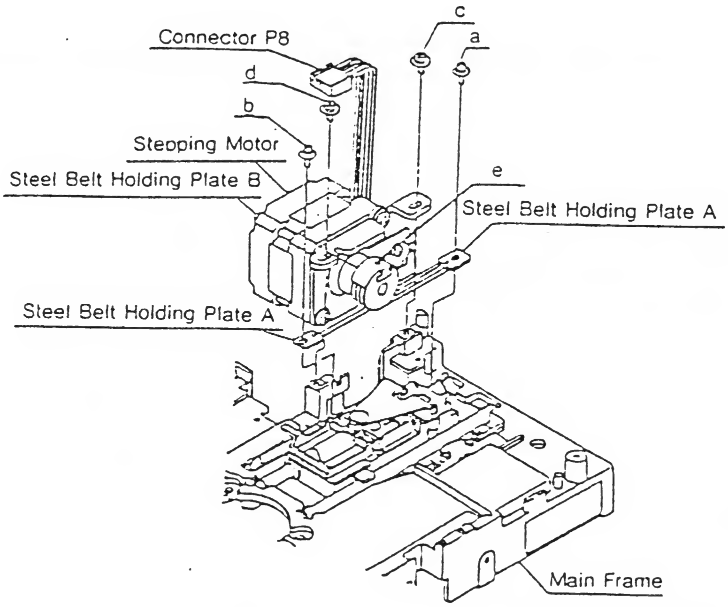

c
Connector P8
a
d
b
Steoping Motor
Steel Belt Holding Plate B
e
Steel Belt Holding Plate A
Steel Belt Holding Plate A
Main Frame

FIGURE 5-41. STEPPING MOTOR

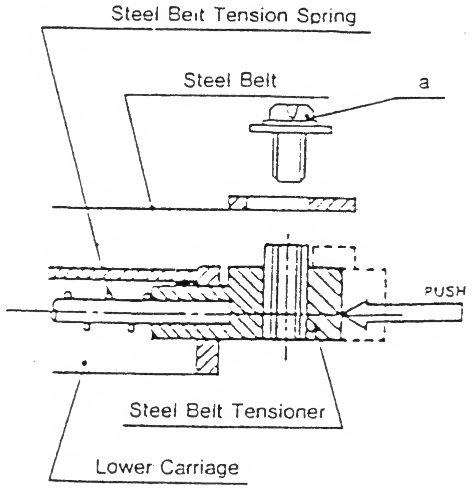


FIGURE 5-42. STEEL BELT TENSIONER

Assembly

1) Set the steel belt on the stepping motor pulley, and fasten the steel belt holding plate B by tightening the setscrew (e) provisionally.

   (Screw tightening torque : about 1.5 kg.cm)

2) Tighten the stepping motor bracket setscrews (c) and (d) provisionally to fix the stepping motor to the main frame.

   (Screw tightening torque : about 4.0 kg.cm)

3) Set the steel belt holding plate B (front edge) on the lower carriage, and tighten the setscrew (b) provisionally.

   (Screw tightening torque : about 2.0 kg.cm)

4) Attach the steel belt holding plate A (back edge) to the steel belt tensioner by pushing the steel belt tensioner towards lower carriage, and fasten the steel belt against the steel belt tensioner.

   (Screw tightening torque : about 4.0 kg.cm)

5) Position the belt line connecting the steel belt holding plates A and B in parallel with the slide shaft, and then tighten the setscrews (b) and (c) securing the steel belt holding plates A and B.

   (Screw tightening torque : b: about 4.0 kg.cm, e : about 2.5kg.cm)

   Note : ● By moving the carriage manually, check to make sure the movement is smooth without abnormal noise or broken or bent belt.

6) Set the jacket lifter spring.

7) Catch the stepping motor lead wire by the lead wire clamps of the motor bracket and the main frame, and connect the stepping motor lead wire connector P8 to the motor circuit board connector J8.

Note : ● Wire in such a way that the steel belt tensioner does not come in contact with the stepping motor lead wire.

8) Mount the subframe unit.

9) Attach the main circuit board shield plate.

10) Attach the clamp lever.

11) Mount the main circuit board.

12) Adjust the off-track sensor, the index sensor and the track 00 sensor positions.

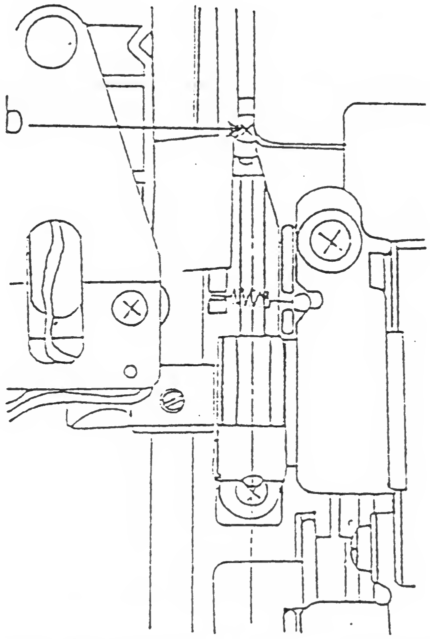


FIGURE 5-43. STEEL BELT POSITION

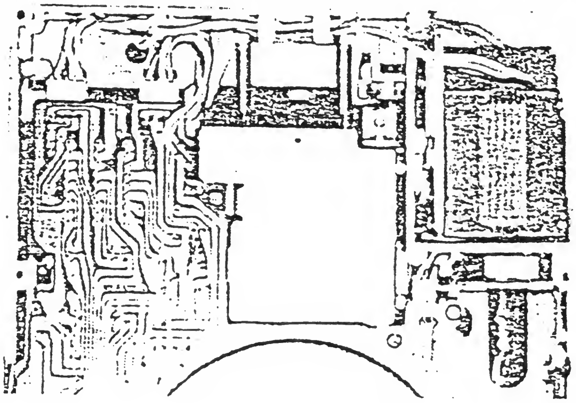


FIGURE 5-44. LEAD WIRE WIRING

5.6.13 Head Carriage Unit

Disassembly

1) Dismount the main circuit board unit.
2) Take off the clamp lever.
3) Take off the main circuit board shield plate.
4) Dismount the subframe unit.
5) Remove the jacket lifter spring.
6) Dismount the stepping motor unit.
7) Disconnect the head wire from the joint on the main frame.
8) Remove the slide shaft holding plate.
9) Remove the head carriage unit, the slide shafts A and B and the jacket lifter from the main frame.

* Move the carriage near the center of the movable part, raise the track 00 sensor (slide shaft B) and then take up the whole carriage unit.

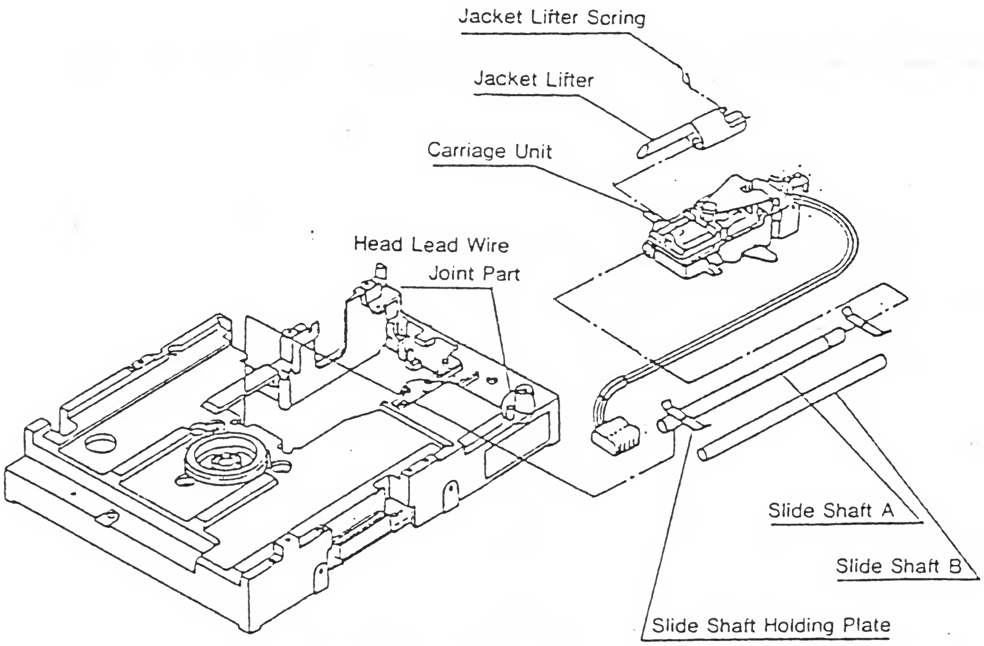


FIGURE 5-45. HAED CARRIAGE UNIT

Assembly

1) Set the head carriage unit, slide shafts A and B and jacket lifter, and mount them on the main frame by means of the slide shaft holding plate.
2) Attach the head lead wire to the main frame and bond it with Cemedine # 575.

   Notes :
   - The head lead wire must not get tensed when the carriage moves to the innermost track.
   - The head lead wire must not slip out of the slide guide rail at the outermost track.
3) Mount the stepping motor unit.
4) Set the jacket lifter spring.
5) Mount the subframe unit.

   Note : Place the upper carriage arm on the collet lever.
6) Mount the main circuit board shield plate.
7) Attach the clamp lever.
8) Mount the main circuit board unit.
9) Adjust the head load lever, off-track, index and track 00 sensor positions.

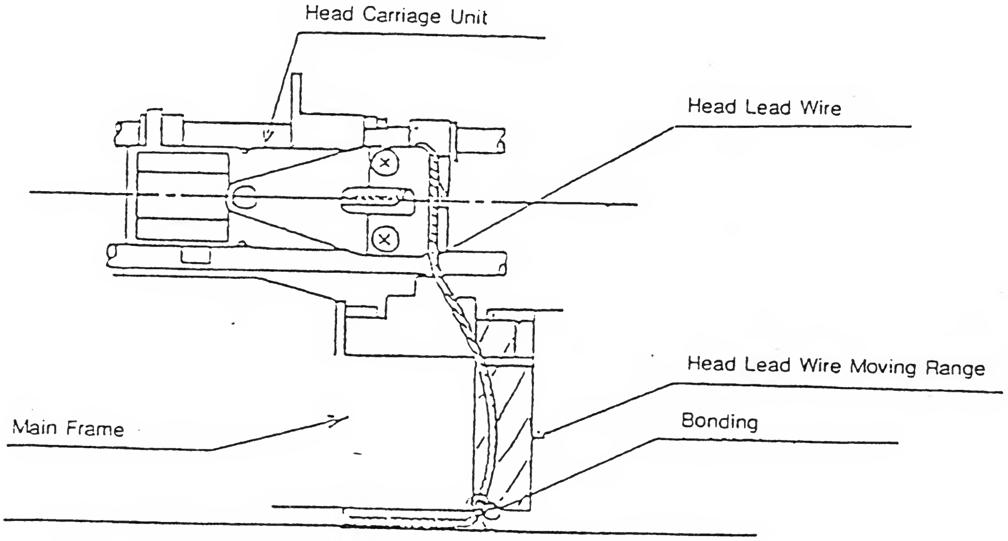


FIGURE 5-46. HAED CARRIAGE UNIT

5.7 MDD-531 DISASSEMBLY AND ASSEMBLY

5.7.1 Replacement of Front Panel

Removal	1. Loosen the clamp screws (4 pcs.) and remove the front panel.
Mounting	1. Mount a new front panel with clamp screws (4 pcs.).
Adjustment after replacement	1. Adjustment of the button gap.

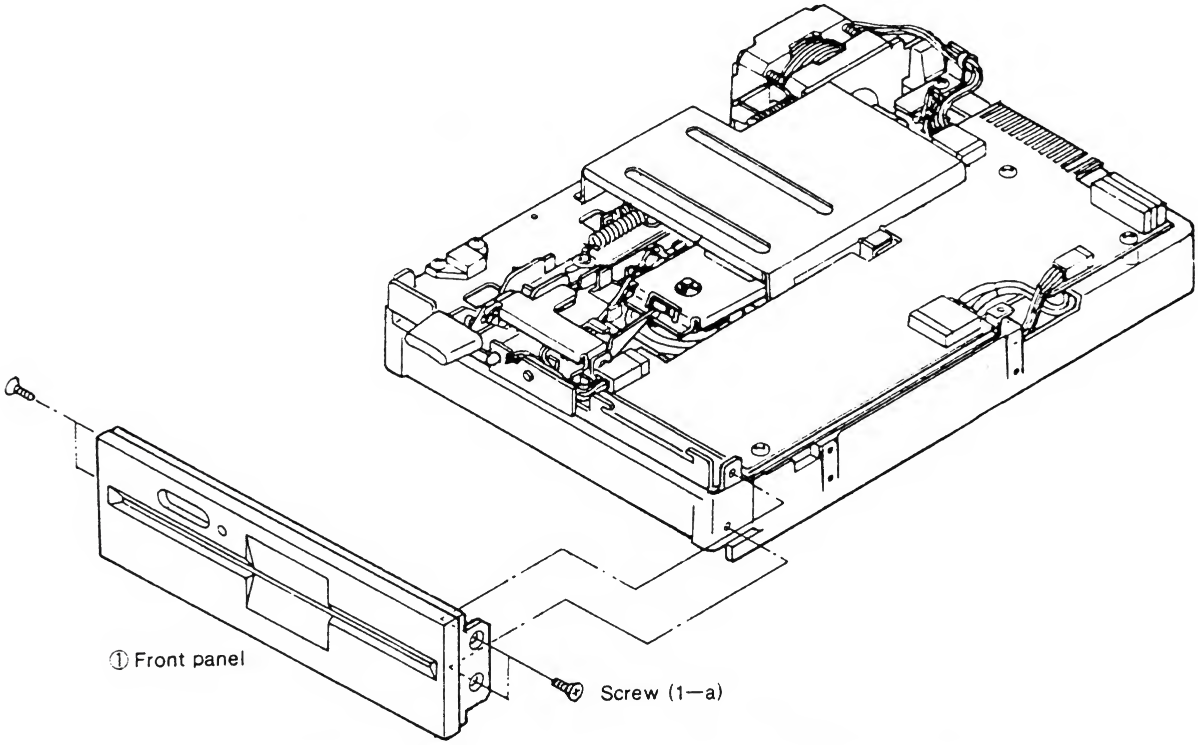


FIGURE 5-47. REPLACEMENT OF FRONT PANEL

5.7.2 Replacement of Main PCB Assembly

Removal	1. Pull out connectors J3, J4, J5 and J6 from the main PCB assembly. 2. Remove the main PCB assembly after removing mounting screws 1 (1 pc.) and 2 (2 pcs.). Pay attention so that the spacers colars used between the PCB assembly and the chassis base (dicast base) will not be lost.
Mounting	1. Install a new main PCB assembly following steps 1 and 2 above in reverse order. 2. Insert each connector.
Adjustment after replacement	1. Confirmation of playback output. 2. Adjustment of asymmetry. 3. Adjustment of Erase off delay.

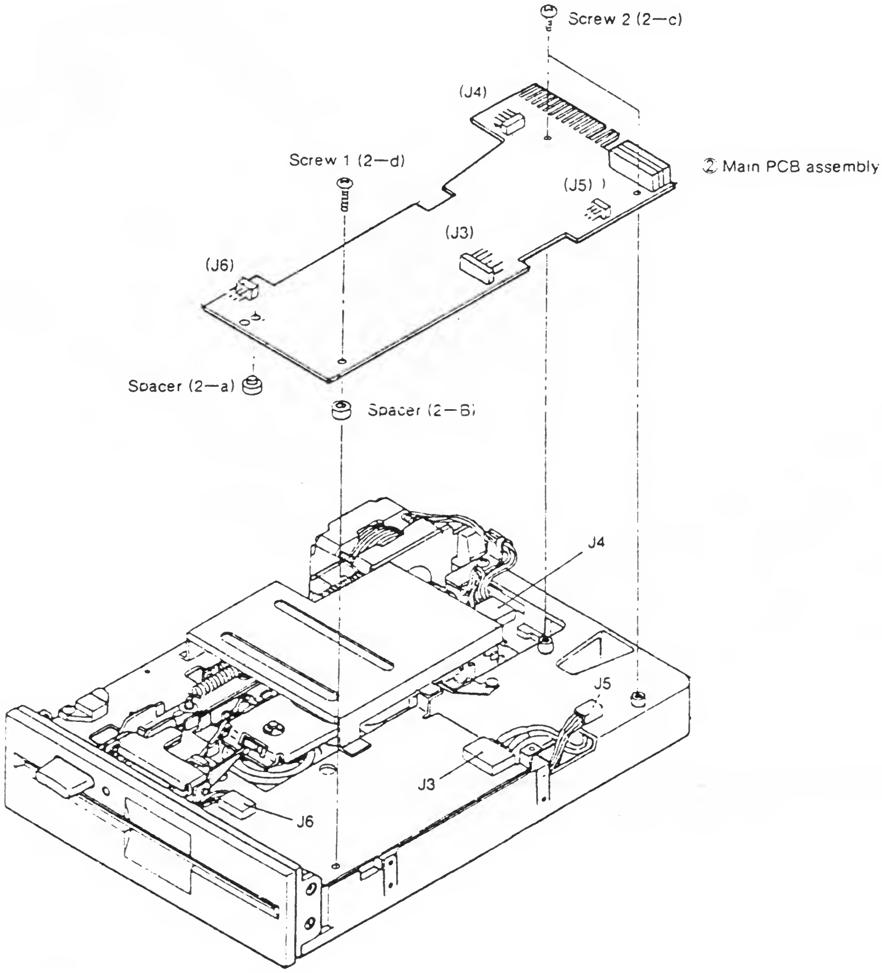


FIGURE 5-48. REPLACEMENT OF MAIN PCB ASSEMBLY

5.7.3 Repacement of Shield Plate

Removal	1. Remove the screws (2 pcs.) and the shield plate.
Mounting	2. Install a new shield plate and place screw locks on the screws.
Adjustment after replacement	None.

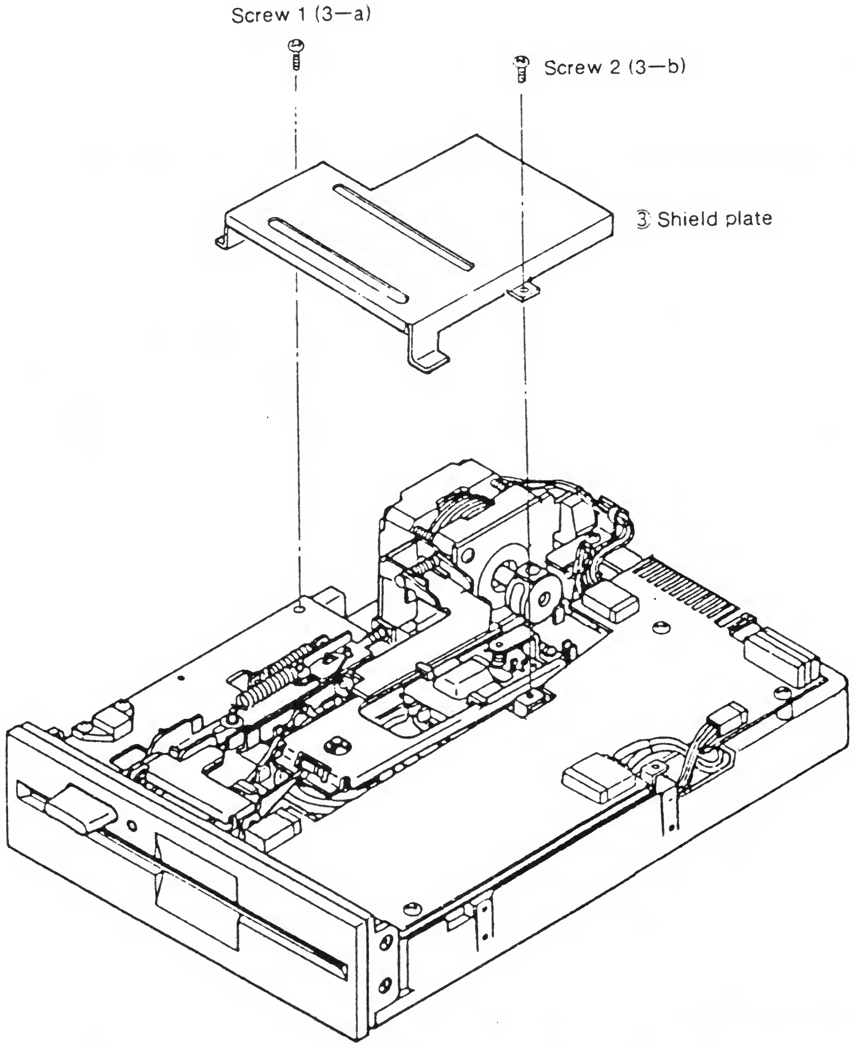


FIGURE 5-49. REPLACEMENT OF SHIELD PLATE

5.7.4 Replacement of Track 00 Photocoupler Assembly

Removal	1. Pull out connector J4 from the main PCB assembly after cutting off the bundle wire band. 2. Separate the pins of the Track 00 photocoupler assembly from connector J4. 3. Remove the Track 00 photocoupler assembly after removing its screws.
Mounting	1. Install a new track 00 photocoupler assembly temporarily. 2. Insert the pins into connector J4 and insert the connector into the main PCB assembly. 3. Tighten the screws after adjustments. 4. Tie up the wires in a bundle.
Adjustment after replacement	1. Adjustment of the track 00 position.

Use tweezers to lift the stoppers on the connector before pulling out the pins

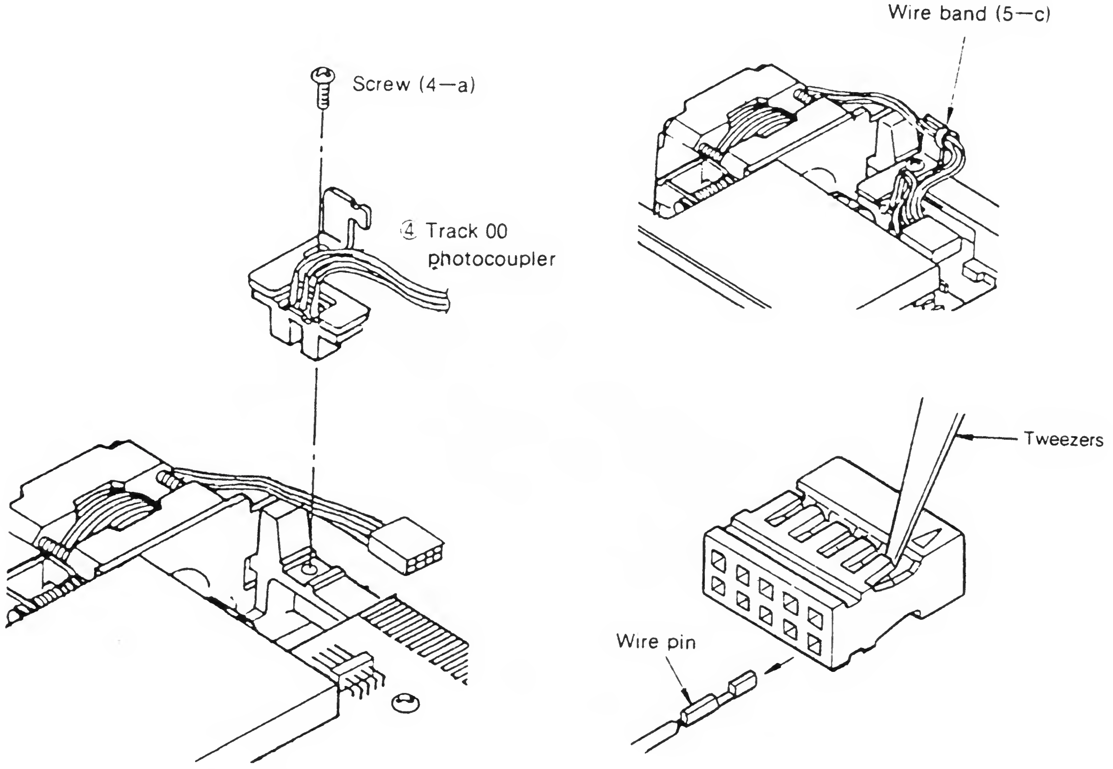


FIGURE 5-50. REPLACEMENT OF TRACK 00 PHOTOCOUPLER ASSEMBLY

5.7.5 Replacement of Steel Belt Assembly

Removal	1. Remove the shield plate. 2. Remove the track 00 photocoupler assembly. 3. Remove the belt clamp screw and mounting screws 1; thereafter, use tweezers to detach the steel belt from the pulley. 4. Remove mounting screw 2 and detach the steel belt assembly from the head assembly.
Mounting	1. Install new steel belt assembly with screw 2 (5-c) 2. Make the correct loop as shown in Fig. 5-51, place it over the pulley and lightly tighten belt clamp screw (5-b) through belt retainer (5-a). 3. Fully tighten clamp screw 1 (5-c) and lever the other end of the steel belt onto the two projections on the head (Fig. 5-51). and then fully secure screw 1 (5-c). 4. Run the head carriage back and forth several times untill the 3 belt sections run smoothly parallel. Now fully tighten belt clamp screw (5-b). 5. Install the Track 00 photocoupler assembly. 6. Install the shield plate.
Adjustment after replacement	1. Adjust the track position. 2. Adjustment the track 00 positioning.

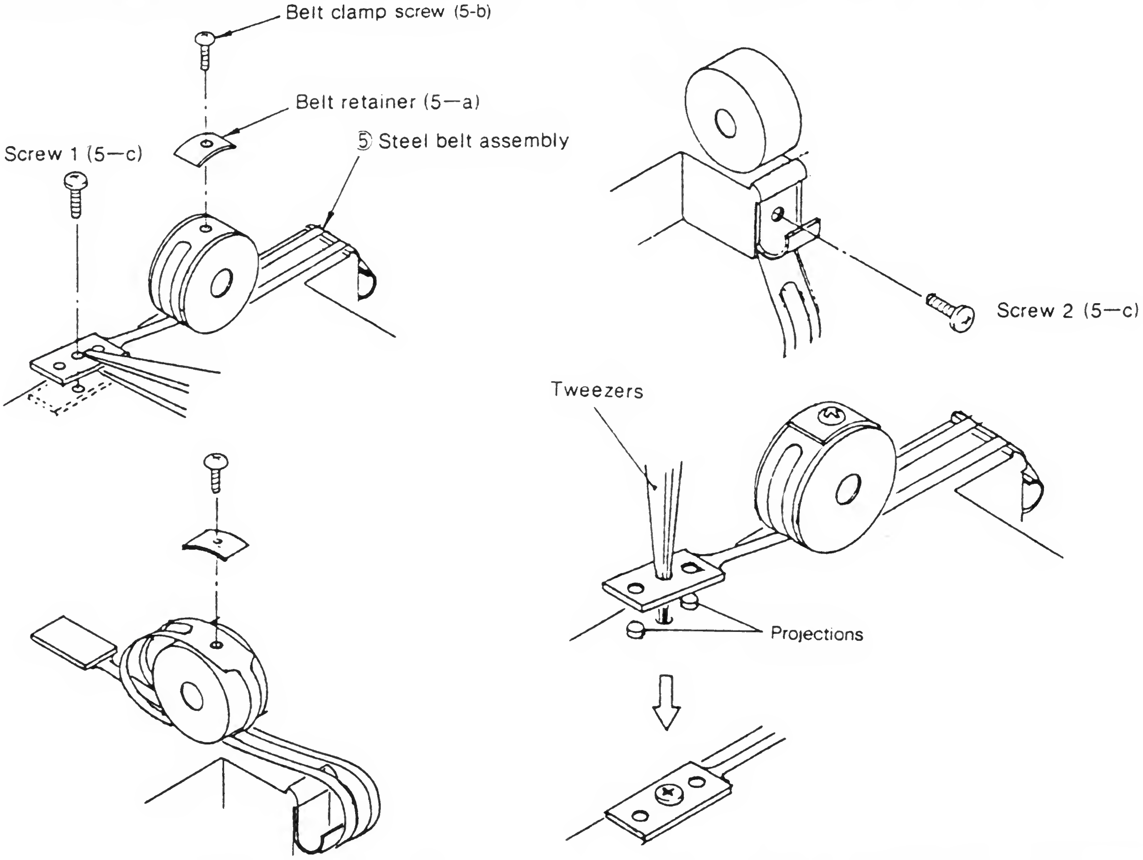


FIGURE 5-51. REPLACEMENT OF STEEL BELT ASSEMBLY

5.7.6 Replacement of Step Motor Assembly

Removal	1. Remove the shield plate. 2. Remove the track 00 photocoupler assembly. 3. Remove the steel belt assembly. 4. Remove the step motor assembly after removing step motor assembly mounting screw 2.
Mounting	1. Install a new step motor (temporalily) with its screws (2 pcs.). 2. Mount the steel belt assembly. 3. Mount the track 00 photocoupler assembly. 4. Mount the shield plate. 5. Tighten the screws after adjustments.
Adjustment after replacement	1. Adjustment of the track position.

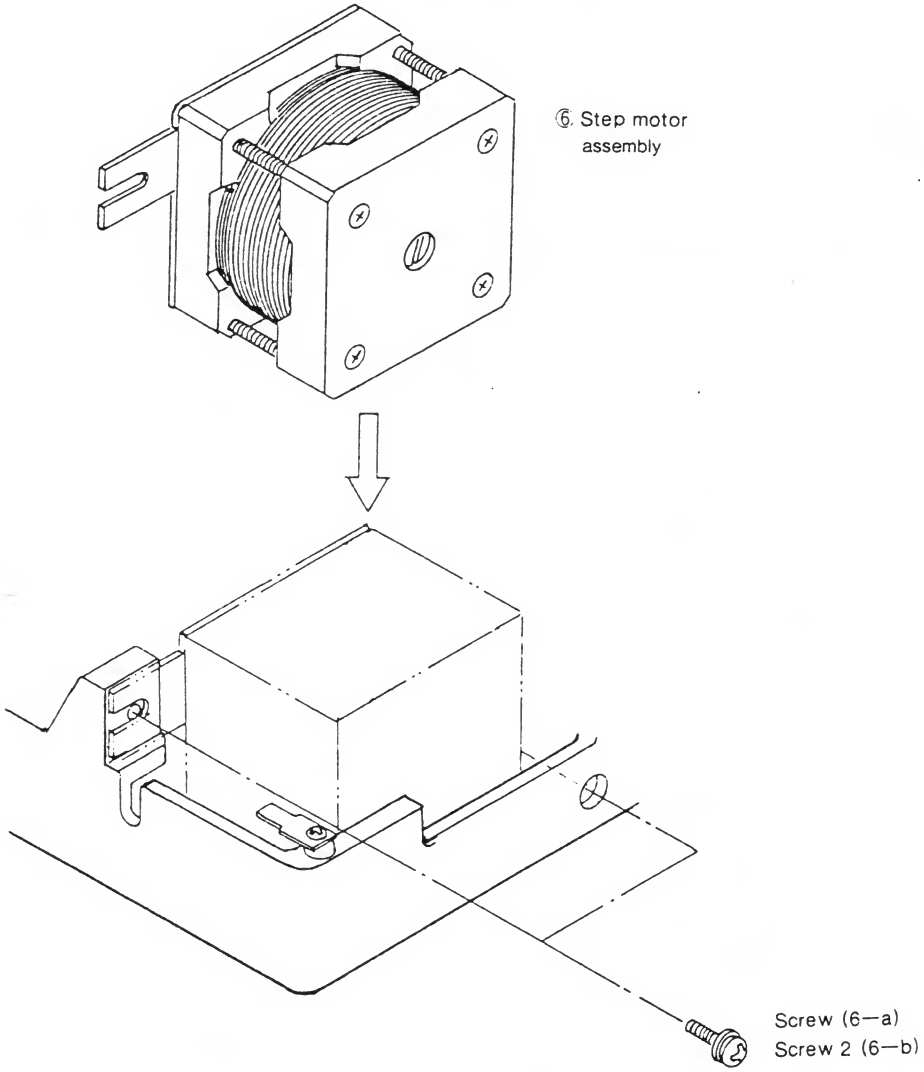


FIGURE 5-52. REPLACEMENT OF STEP MOTOR ASSEMBLY

5.7.7 Replacement of Head Assembly

Removal	1. Remove the shield plate. 2. Remove the track 00 photocoupler assembly. 3. Remove the steel belt assembly. 4. Pull out connection J3 and cut off the bundle wireband. 5. Remove the head assembly after loosing the double clamp screws and pull out the guide bars (2 pcs.).
Mounting	1. Install the head assembly so that the head arm of the new head assembly will be positioned on the head load arm. 2. Fix the guide bars by tightening the double clamp screws after inserting guide bars through the head assembly. Note: Adjust the guide bars to the face of the die cast base. 3. Fix the head cable with a bundle wire band. 4. Apply the Lubriplate Aero to the guide bars and move the head back and forth to make sure that the movement of the head assembly is smooth. 5. Install each part removed in reverse order.
Adjustment after replacement	1. Adjustment of the index burst position. 2. Confirmation of the reproduced output. 3. Adjustment of the track position. 4. Adjustment of the track 00 position. 5. Adjustment of the 0-1 head clearance. ※ Only for use with a head load solenoid. 6. Confirmation of the modulation.

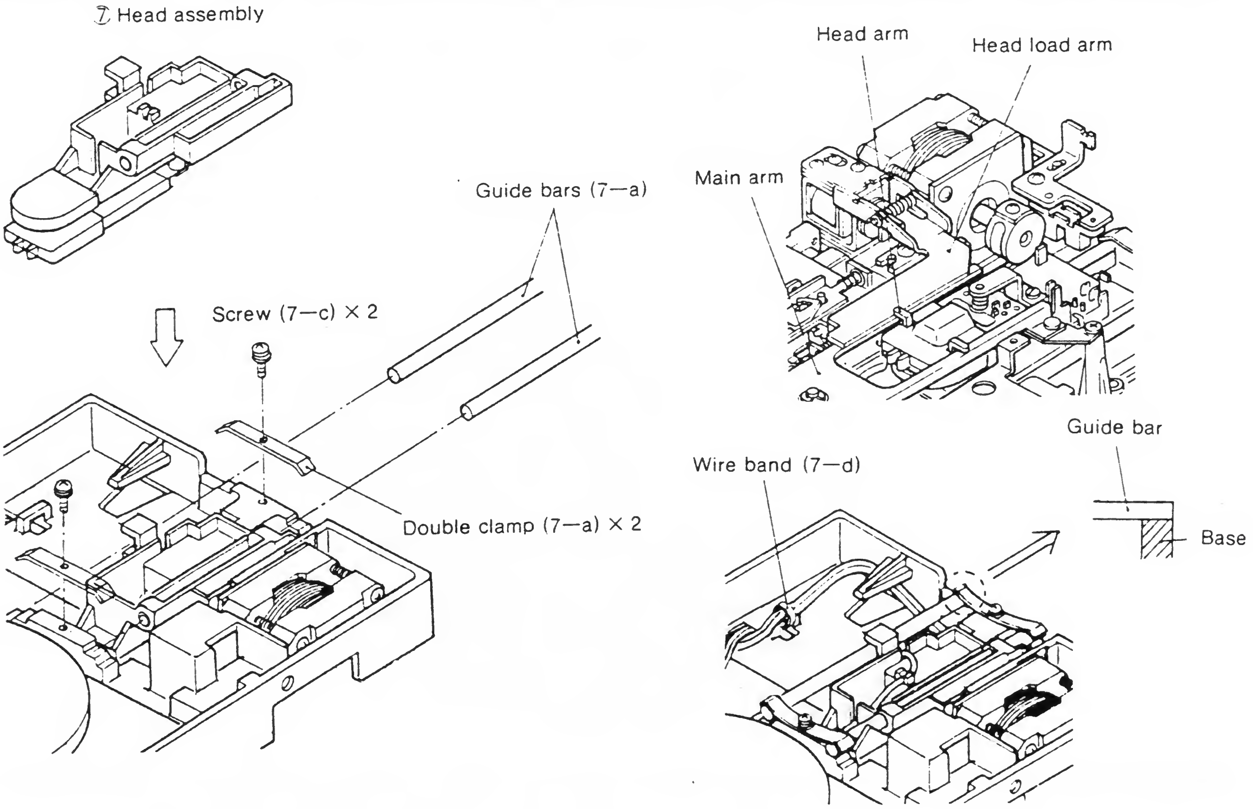


FIGURE 5-53. REPLACEMENT OF HEAD ASSEMBLY

5.7.8 Replacement of Head Load Arm Mounting Assembly

Removal	1. Remove the shield plate. 2. Remove the head load arm mounting assembly after removing the screws (2 pcs.).
Mounting	1. Install a new head load arm mounting assembly after inserting the head load arm between the main arm and the head arm. 2. Install the shield plate.
Adjustment after replacement	None.

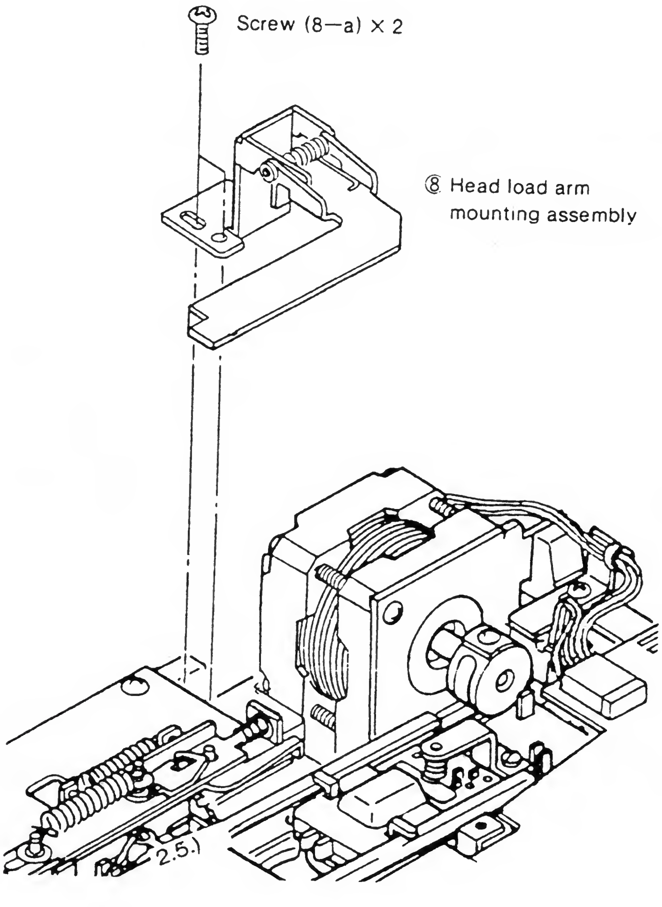


FIGURE 5-54. REPLACEMENT OF HEAD LOAD ARM MOUNTING ASSEMBLY

5.7.9 Replacement of Write Protect Photocoupler

Removal	1. Remove the DD motor FPC from the write protect photocoupler using a soldering iron. 2. Remove the write protect photocoupler after removing its screws.
Mounting	1. Install a new photocoupler with mounting screws. 2. Solder the DD motor FPC onto the photocoupler. 3. Cut the pins to the correct length on the photocoupler assembly.
Adjustment after replacement	1. Confirmation of the WRITE PROTECT signal.

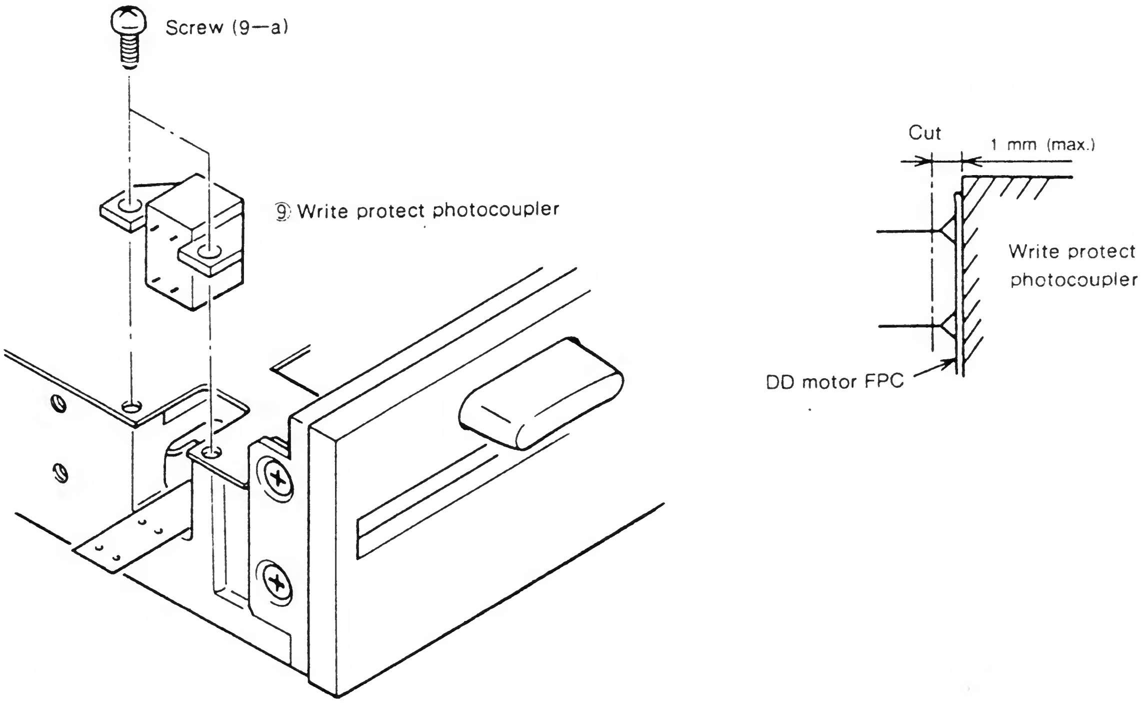


FIGURE 5-55. REPLACEMENT OF WRITE PROTECT PHOTOCOUPLER

5.7.10 Replacement of Phototransistor Holder Assembly

Removal	1. Remove the front panel. 2. Pull out pin J6 and wire pins from the phototransistor holder assembly. 3. Pull out the lead wire from the phototransistor assembly after loosening the screws for the LED PCB assembly. 4. Remove the phototransistor holder assembly after removing its screws.
Mounting	1. Install a new assembly with its screw temporarily tightened. 2. Tighten the screw on the LED PCB assembly wire holder after positioning the lead wire behind it. 3. Insert wire pins into the connector and then into J6. 4. Place a screw lock on the screw after adjustment. 5. Install the front panel.
Adjustment after replacement	1. Adjust the index burst position.

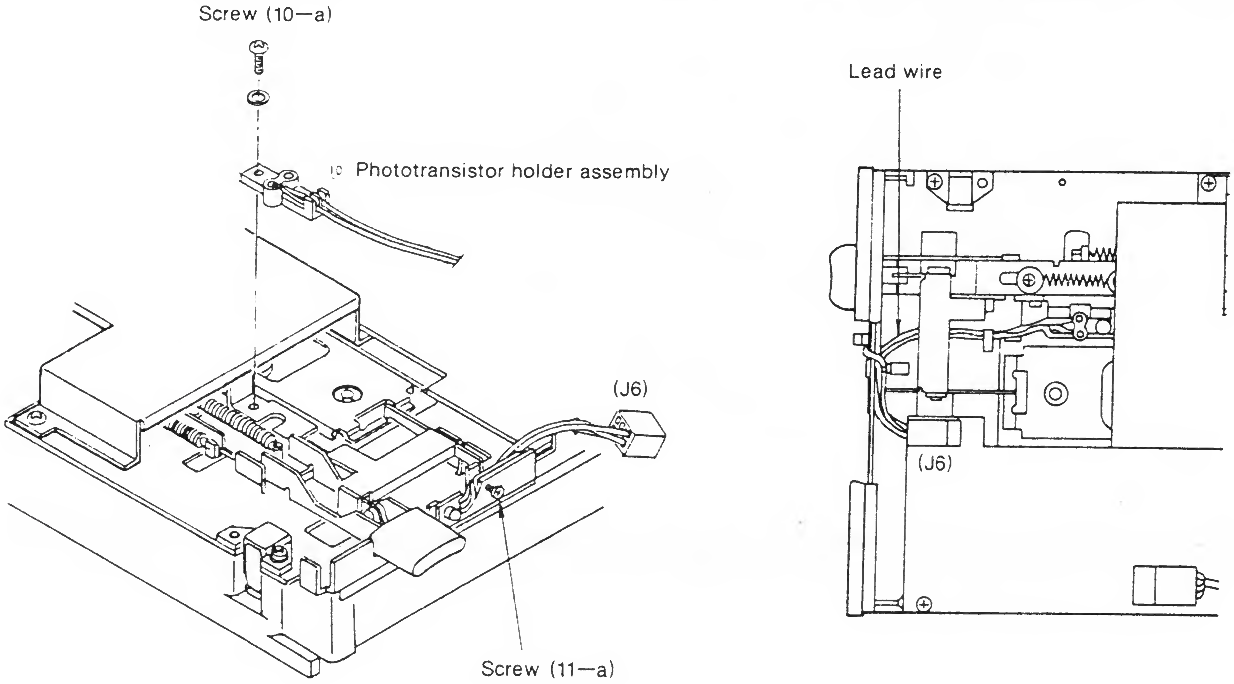


FIGURE 5-56. REPLACEMENT OF PHOTOTRANSISTOR HOLDER ASSEMBLY

5.7.11 Replacement of LED PCB Assembly

Removal	1. Remove the front panel. 2. Pull out the LED PCB assembly pins from connector J6. 3. Remove the LED PCB assembly after removing its screws.
Mounting	1. Install a new LED PCB assembly. Note: Be sure to position the wires under the mounting screw (wire holder). 2. Insert the pins into connector J6 and insert it into the PCB assembly. 3. Mount the front panel.
Adjustment after replacement	1. Confirm the action of the LED.

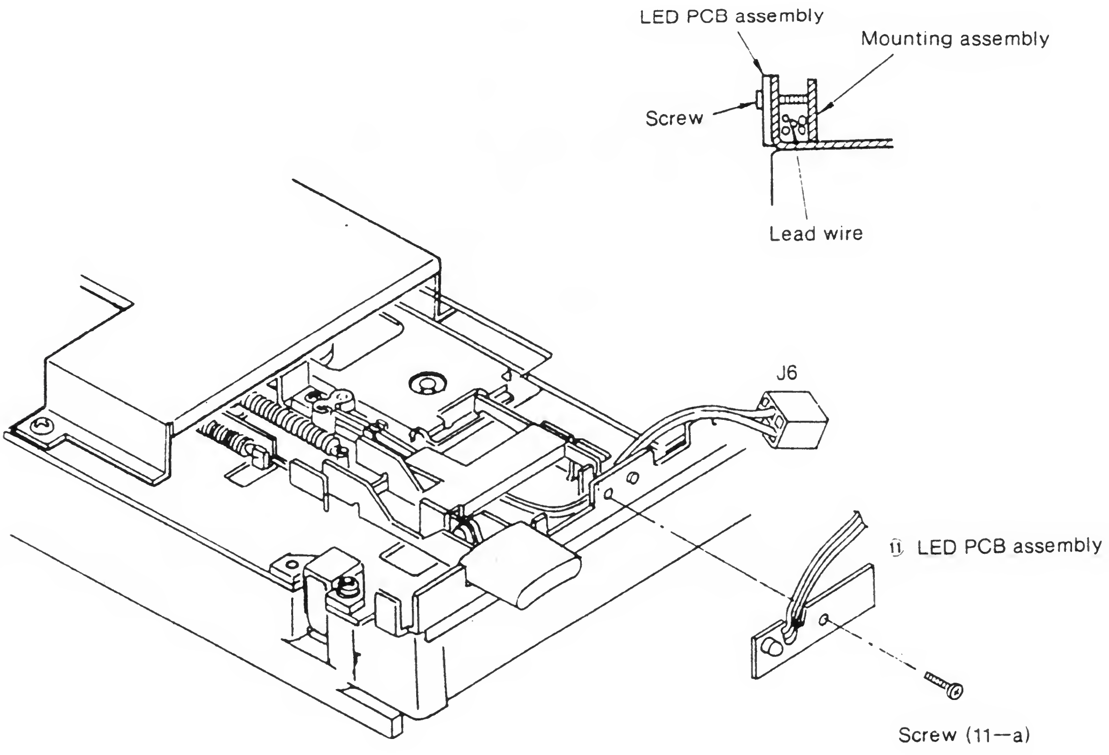


FIGURE 5-57. REPLACEMENT OF LED PCB ASSEMBLY

5.7.12 Replacement of Push Button

Removal	1. Remove the front panel. 2. Pull out the button from the mounting plate assembly.
Mounting	1. Install a new button. 2. Install the front panel.
Adjustment after replacement	1. Confirm the button gap.

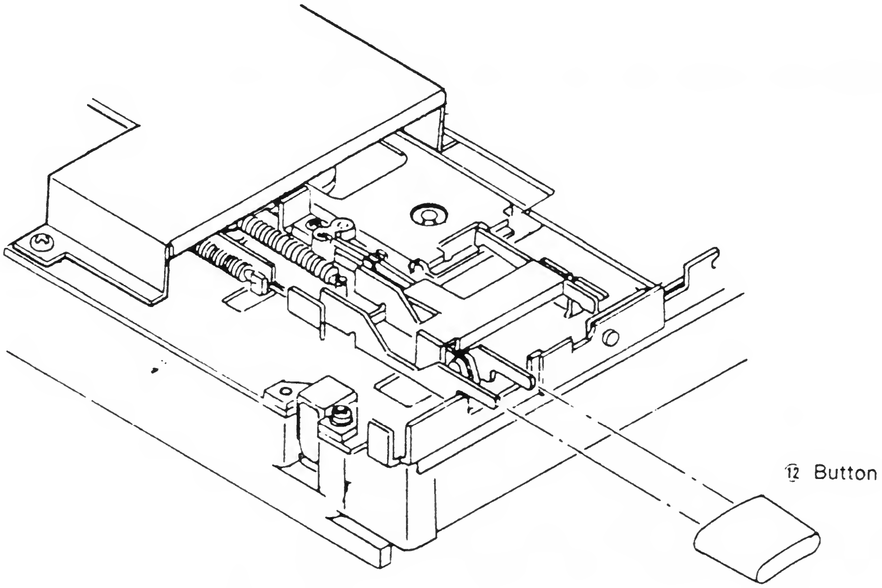


FIGURE 5-58. REPLACEMENT OF PUSH BUTTON

5.7.13 Replacement of Mounting Plate Assembly

Removal	1. Remove the front panel. 2. Remove the main PCB assembly. 3. Remove the shield plate. 4. Remove the write protect photocoupler screw (1 pc.). 5. Remove the phototransistor holder assembly. 6. Remove the LED PCB assembly. 7. Remove the push button. 8. Remove the screws (2 pcs.) and the mounting plate assembly.
Mounting	1. Insert a new mounting plate assembly. 2. Insert each part in reverse order.
Adjustment after replacement	1. Adjustment of the index burst position. 2. Confirmation of the button gap.

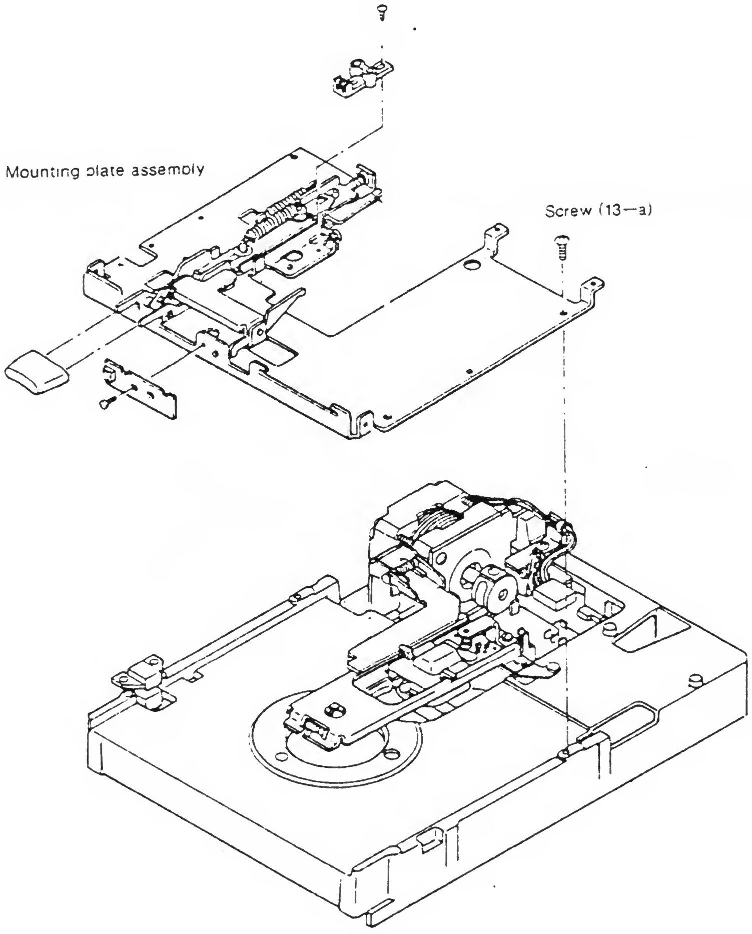


FIGURE 5-59. REPLACEMENT OF MOUNTING PLATE ASSEMBLY

5.7.14 Replacement of Main Arm Assembly

Removal	1. Remove the main PCB assembly. 2. Remove the shield plate. 3. Remove the mounting plate assembly while keeping the button, LED PCB assembly, and phototransistor holder assembly intact. 4. Remove the main arm assembly after removing its screws and washers.
Mounting	1. Mount the new main arm assembly; align the center cone and the center of the spindle and, thereafter, apply a screw lock to the mounting screws. 2. Install the mounting plate assembly. 3. Install the main PCB assembly.
Adjustment after replacement	1. Adjustment of the track position. 2. Confirmation of modulation. 3. Confirmation of the clamp mechanism.

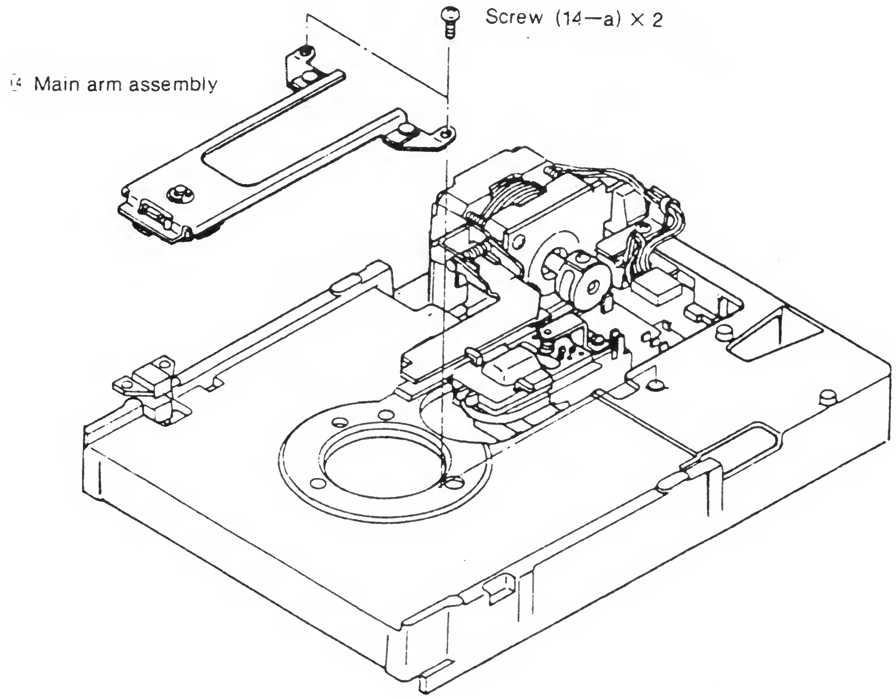


FIGURE 5-60. REPLACEMENT OF MAIN ARM ASSEMBLY

5.7.15 Replacement of DD Motor

Removal	1. Remove the main PCB assembly. 2. Remove the DD motor FPC from the write protect photocoupler. 3. Pull out the DD motor cable assembly. 4. Remove the DD motor after removing screws 1 (2 pcs.) and 2 (1 pcs.).
Mounting	1. After fitting a new DD motor, tighten screws 1 and 2, in the order named. 2. Insert the DD motor cable assembly. 3. Install each part with its screws in reverse order.
Adjustment after replacement	1. Adjustment of the index burst. 2. Adjustment of the track positioning. 3. Confirmation of the WRITE PROTECT signal. 4. Confirmation of modulation. 5. Confirmation of the clamp mechanism action.

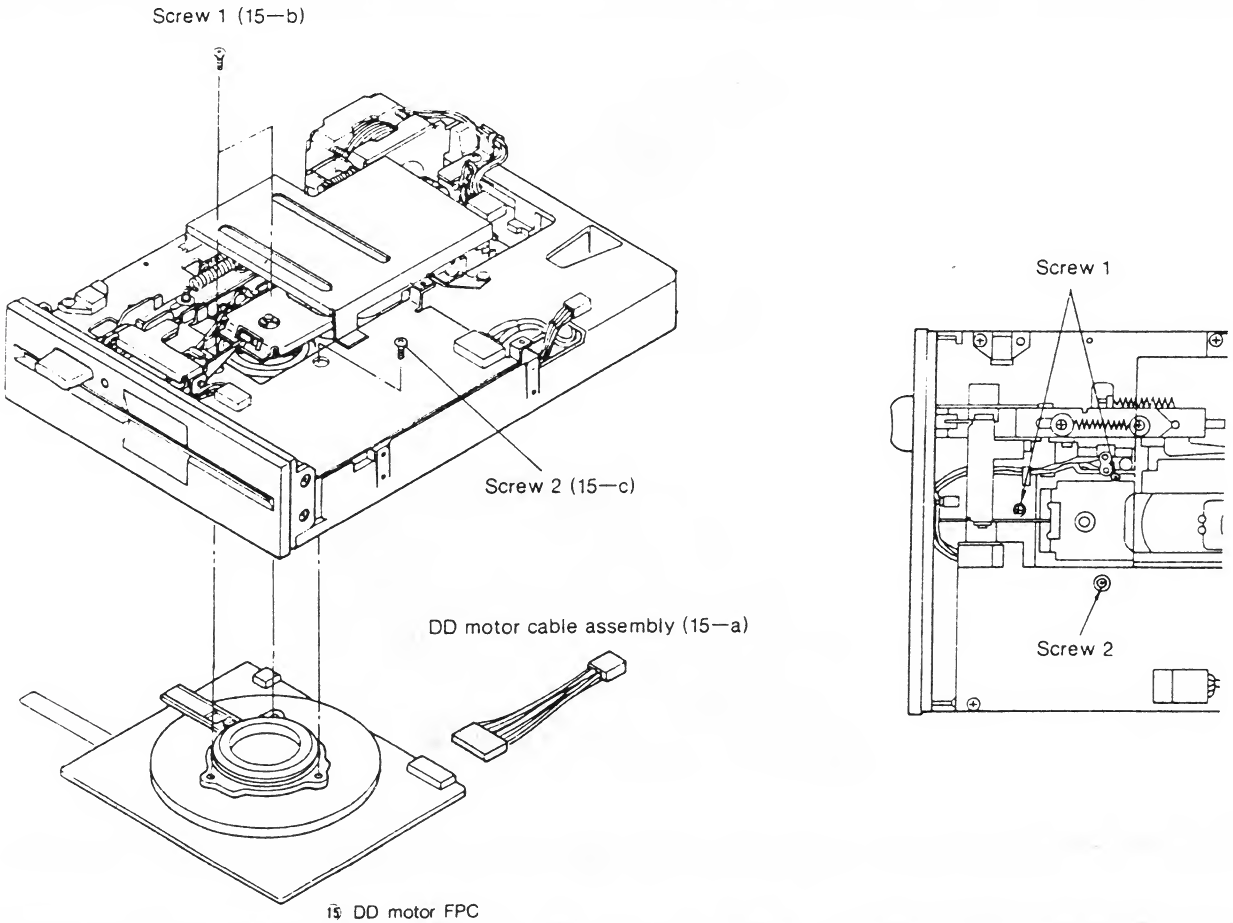


FIGURE 5-61. REPLACEMENT OF DD MOTOR

5.7.16 Replacement of Head Load Arm Assembly (Option)

Removal	1. Remove the shield plate. 2. Remove the head load arm assembly from the head load solenoid after removing its screws.
Mounting	1. Install a new head load arm assembly onto the head load solenoid and temporarily tighten its screws. 2. Confirm the action of the head load solenoid. 3. Adjust the gap between the side 0 head and side 1 head with reference to the mounting location of the head load arm assembly while keeping it clamped without a disk ; tighten the screws and apply a screw lock. 4. Install the shield plate.
Adjustment after replacement	1. Adjust the 0-1 head gap.

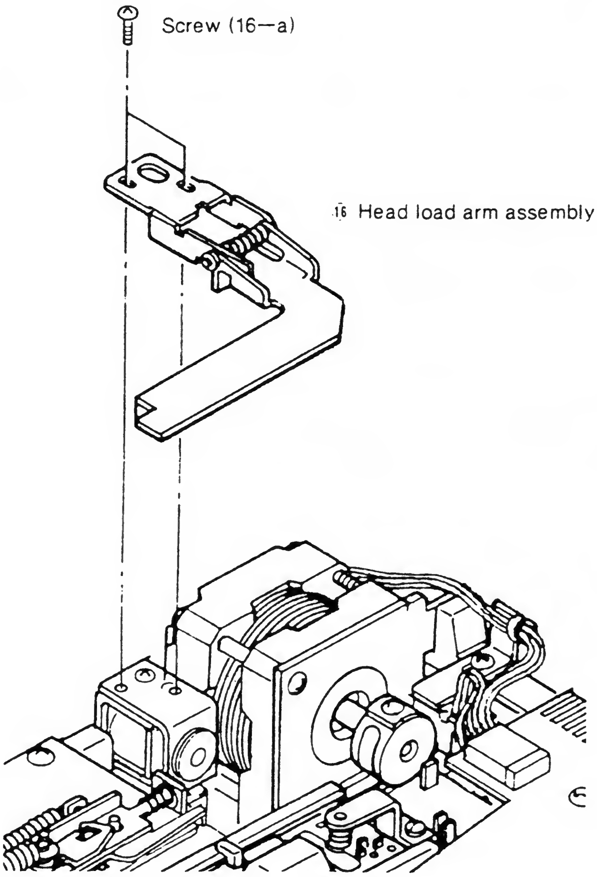


FIGURE 5-62. REPLACEMENT OF HEAD LOAD ARM ASSEMBLY

5.7.17 Replacement of Head Load Solenoid Assembly (Option)

Removal	1. Remove the shield plate. 2. Pull out the connector from the DD motor. 3. Remove the head load arm assembly. 4. Remove the solenoid assembly after removing its screws (2 pcs.).
Mounting	1. Install a new solenoid assembly after passing its leads through the hole in the base. 2. insert the connector into the DD motor. 3. Install the head load arm assembly. 4. Install the shield plate.
Adjustment after replacement	1. Adjust the 0–1 head gap.

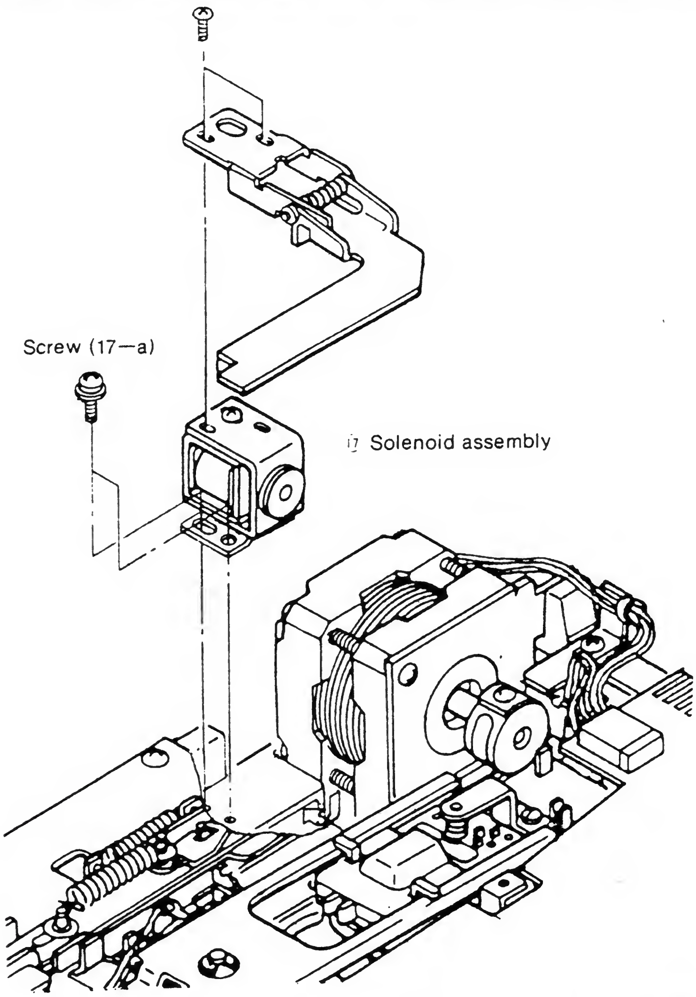


FIGURE 5-63. REPLACEMENT OF HEAD SOLENOID ASSEMBLY

CHAPTER

6

ADJUSTMENT AND MAINTENANCE

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6.1 ADJUSTMENT AND MAINTENANCE OVERVIEW

The SD-521 disk drives are the only system components requiring adjustmemt. The disk drives are factory-assembled with great precision and should be adjusted following disassembly or part replacement only, as described in Section 6.2. The FMTC disk controller is necessary to adjust the floppy disk drives.

Section 6.3 provides procedures for routine preventive maintenance and cleaning. Lubrication and adhesive application, describes in Section 6.4, are limited to the floppy disk drives.

6.2 SD-521 FLOPPY DISK DRIVE ADJUSTMENT

The following adjustments are necessary for disassembly only; adjustment and measuring tools are listed in Table 6-1. Test points on the control board are used for monitoring signal waveforms during adjustment, as described in Table 6-2; test point locations are diagrammed in Figure 6-1.

TABLE 6-1. FLOPPY DISK DRIVE ADJUSTMENT EQUIPMENT

ITEM	PART NUMBER
Phillips screwdriver (#1)	B743800100
Phillips screwdriver (#2)	B743800200
Flat-blade screwdriver (#1)	B743000100
Torque driver	B740100102
Feeler guage (0.4mm, 0.28mm)	----------
FDD controller (FMTC)	B777900501
Oscilloscope (2 channel)	----------
Frequency counter	----------
Head cleaning disk (5 1/4" wet type)	----------
CE adjustment disk (DYMEK No. 512-11D)	B777700101

TABLE 6-2. SD-521 CONTROL BOARD TEST POINTS

TEST POINT	DESCRIPTION
TP1, pins 1 and 3.	Read amp (uA733C) output and adjustment point for the off-track alignment. A differential waveform with a 180 degree phase shift is read at pins 1 and 3.
TP1, pin 2.	Analog GND used with TP1, pins 1 and 3.
TP2, pins 1 and 3.	Differential amp output. Like TP1, a differential waveform with a 180 degree phase shift is read at pins 1 and 3.
TP2, pin 2.	Analog GND used with TP2, pins 1 and 3.
J2, pin 8.	Index detector output, used for RPM adjustment and as the trigger signal for the off-track and azimuth adjustments.
J2, pins 6,10,12, and 14.	Drive select signals.
J2, pin 26.	Track 00 sensor output.

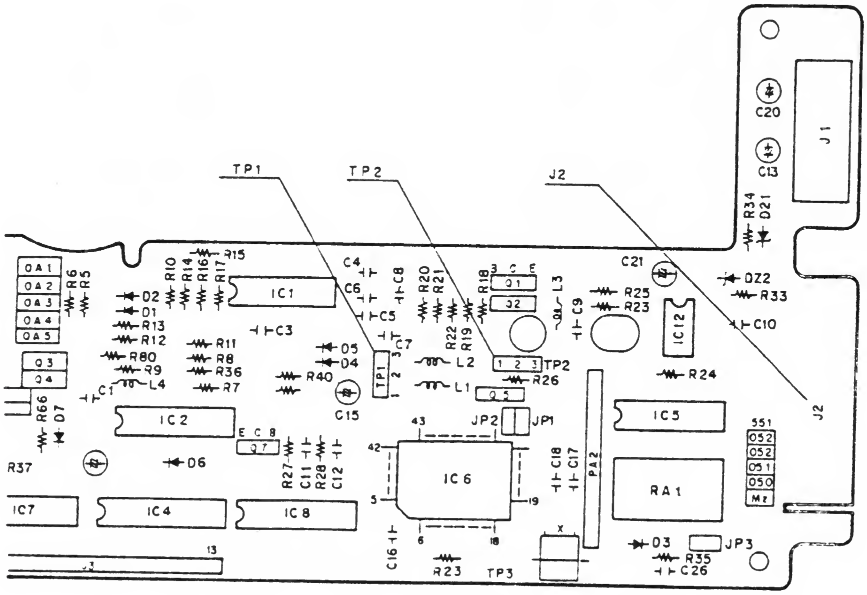


FIGURE 6-1. SD-521 CONTROL BOARD TEST POINT LOCATIONS

6.2.1 Disk Revolution (RPM) Adjustment

The FMTC disk controller with used in the adjustment procedures; connection of the FMTC to the control board is diagrammed in Figure 6-2, and the RPM adjustment procedures are detailed in steps (1) through (6).

1. Connect between the drive and the FMTC as shown in Figure 6-2.

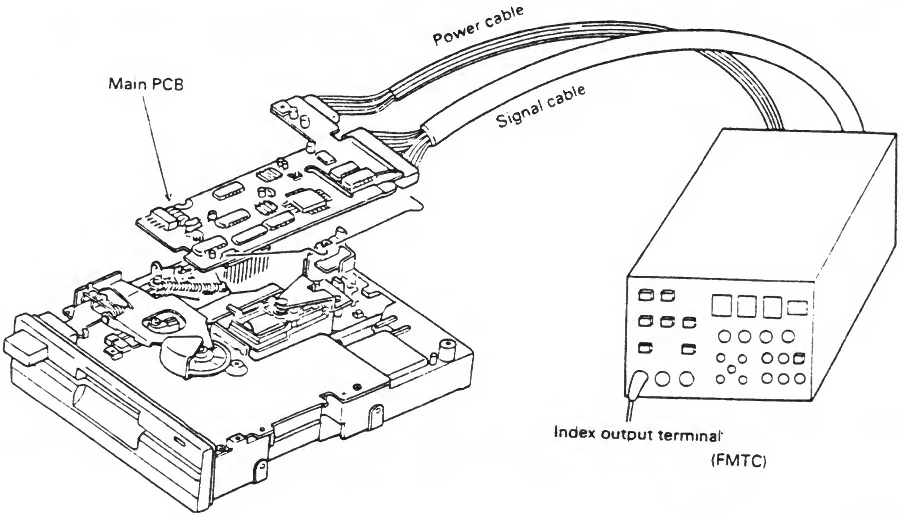


FIGURE 6-2. CONNECTION OF FMTC AND DRIVE

2. Connect the index output terminal of the FMTC to the frequency counter. (Figure 6-3)

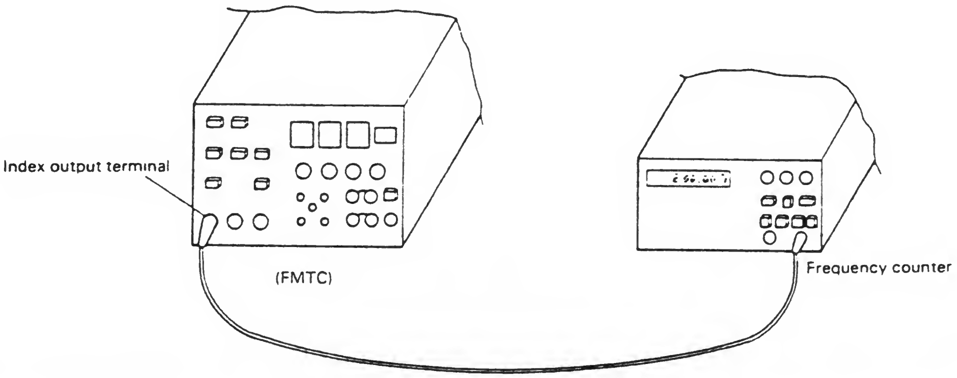


FIGURE 6-3. CONNECTION OF FMTC AND FREQUENCY COUNTER

3. Set the FMTC switch modes as follows:

Motor .... ON
Seek test mode .... OFF
Write enable .... OFF
Step rate .... 6 ms or more
Seek to track 20
Max track 39

4. Insert a blank 5.25-inch floppy disk into the drive to activate the disk drive motor.

5. Set the FMTC to seek track 20. (Figure 6-4)

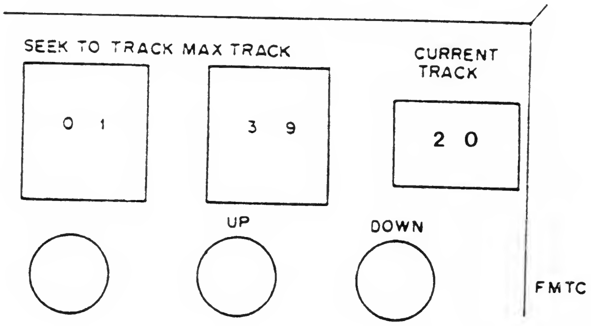


FIGURE 6-4. FMTC PANEL OPERATION

6. Use a flat-blade screwdriver to rotate VR2 on the motor control board until the RPM setting is between 199.7 and 200.3 ms. (Figure 6-5)

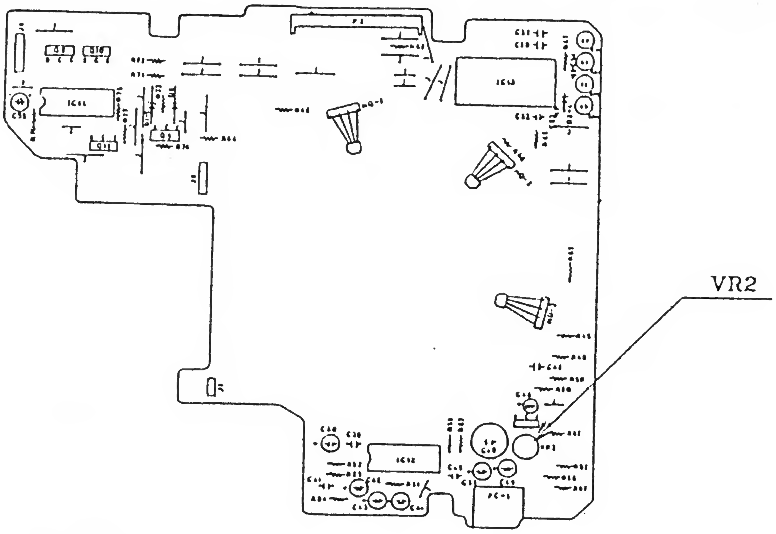


FIGURE 6-5. RPM ADJUSTMENT

* If you connect the index output terminal on the main PC board to the frequency counter, connection is as follows:

FREQUENCY COUNTER	MAIN PC BOARD
INDEX Signal	Pin 5 of IC7
GND Signal	Pin 2 of TP1

6.2.2 Off-Track, Azimuth, and Index Timing Adjustments

NOTE: The off-track, azimuth, and index adjustments differ for the upper and lower heads as follows:

Lower head (Side 0) ..... Off-track and index-timing adjustments can be made. (Adjustment of the azimuth is not possible, but the waveform can be checked.)

Upper head (Side 1) ..... The above three adjustments are performed simultaneously.

Prior to each adjustment, make sure that the disk revolution adjustment has been completed, and prepare the following measuring conditions.

1. Connect both power and signal cables of the FMTC to the main PCB. (Figure 6-6)
2. Connect CH-1 and CH-2 on the oscilloscope to pin 1 and pin 3 of TP1 on the main PCB, respectively.
3. Connect GND on the oscilloscope to pin 2 of TP1 on the main PCB.

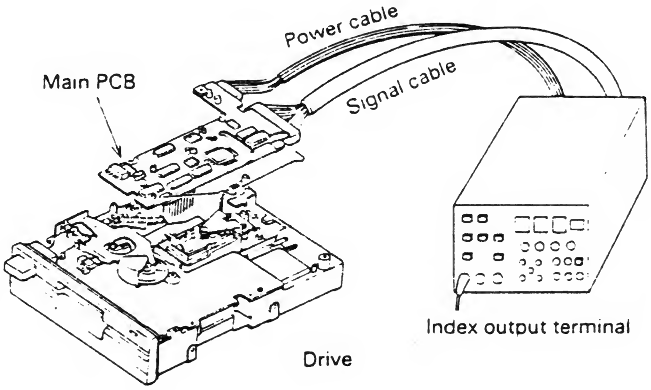


FIGURE 6-6. CONNECTION OF FMTC AND DRIVE

4. Connect the index output terminal on the FMTC to the external trigger input terminal on the oscilloscope.
   (If connecting the external trigger of the oscilloscope to pin 5 of IC7 on the PCB, the trigger edge is "-".)

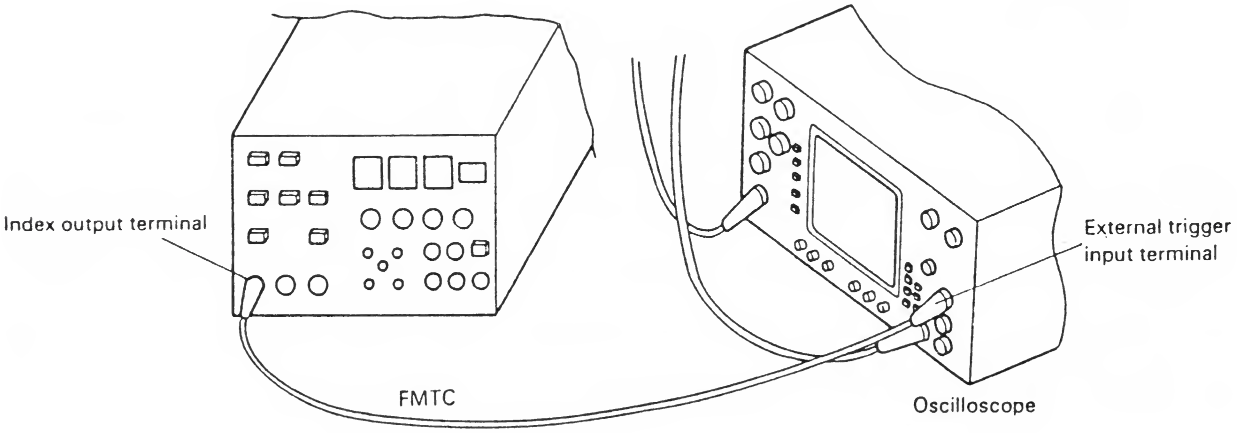


FIGURE 6-7. CONNECTION OF FMTC AND OSCILLOSCOPE

5. Set the oscilloscope as shown in Table 6-3, to adjust side 0, side 1, or both.

TABLE 6-3. OSCILLOSCOPE SETTINGS

SWITCH MODE	OFF-TRACK		AZIMUTH		INDEX TIMING	
	CH-1	CH-2	CH-1	CH-2	CH-1	CH-2
AC-GND-DC	AC	AC	AC	AC	AC	AC
VERT MODE	ADD		ADD		ADD	
INVERT	-	ON	-	ON	-	ON
*VOLTS/DIV	50 mV	50 mV	50 mV	50 mV	50 mV	50 mV
*TIME/DIV	20 ms		0.5 ms		50 us	

* VOLTS/DIV and TIME/DIV should be used in the CAL mode.

6.2.2.1 Side 0 Adjustment

Off-Track Adjustment (Side 0)

1. Set the FMTC to SIDE 0.
2. Turn the FMTC power switch on.
3. Insert the CE disk into the drive to activate the disk drive motor.
4. Turn the DRIVE SELECT switch of the FMTC to ON.
5. Press the CURRENT TRACK push button of the FMTC, and check for an off-track indication on the oscilloscope when the head is moved from track 00 to track 34 and from track 39 to track 34. (Figure 6-8)

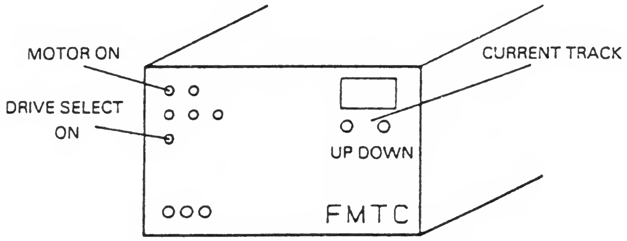


FIGURE 6-8. FMTC OPERATIONS POSITION

6. Observe that the off-track waveform is synchronous with the index signal indicated on the oscilloscope. (Figure 6-9)

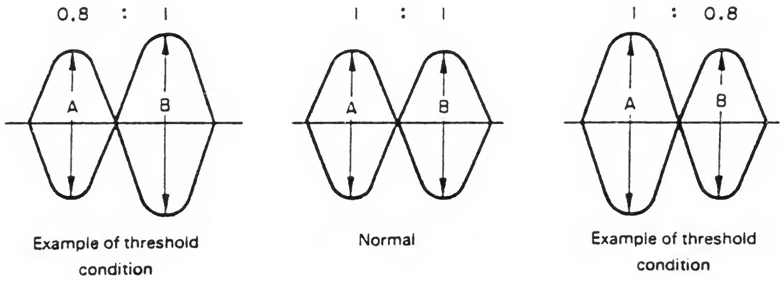

0.8 : 1
A
B
Example of threshold condition
1 : 1
A
B
Normal
1 : 0.8
A
B
Example of threshold condition

FIGURE 6-9. OFF-TRACK WAVEFORM

7. Check whether the following conditions are satisfied, when the head is moved from track 00 to track 34 and from track 39 to track 34,

A : B = 1 : 1 .... Normal
A : B = 1 : 0.8 .... Threshold point
B : A = 1 : 0.8 .... Threshold point

There is no need for adjustment if the off-track waveform ratios are between 0.8 and 1.0.

If these ratios are less than 0.8, adjust them as follows:

1. Loosen the two stepper motor bracket set screws. (Figure 6-10)

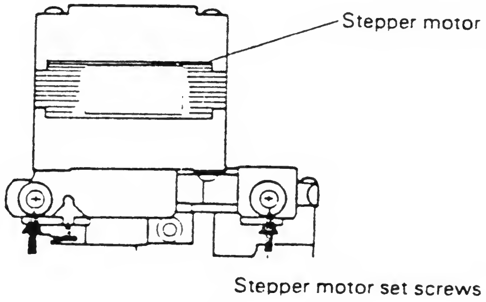
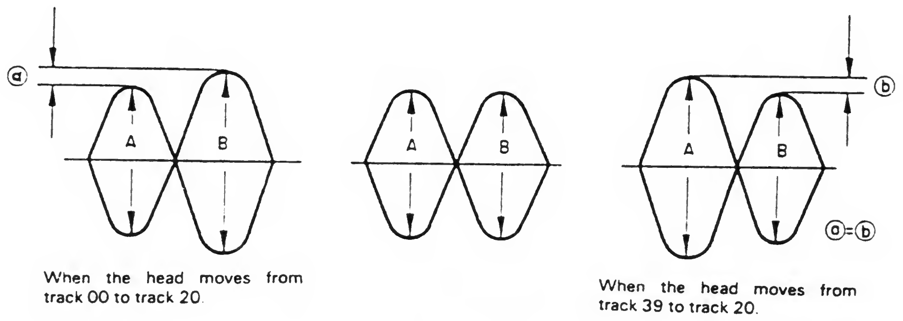


FIGURE 6-10. STEPPER MOTOR POSITION ADJUSTMENT

2. Insert the flat-blade screwdriver into the V slots of the main frame and stepper motor bracket, and rotate the screwdriver to adjust the motor bracket position (Figure 6-12). Observing the patterns indicated on the oscilloscope, adjust the off-track waveform so that the ratio of A to B becomes 1 : 1 or within the specified range. (Figure 6-11)



When the head moves from track 00 to track 20.

When the head moves from track 39 to track 20.

FIGURE 6-11. OFF-TRACK WAVEFORM ADJUSTMENT (SIDE 0)

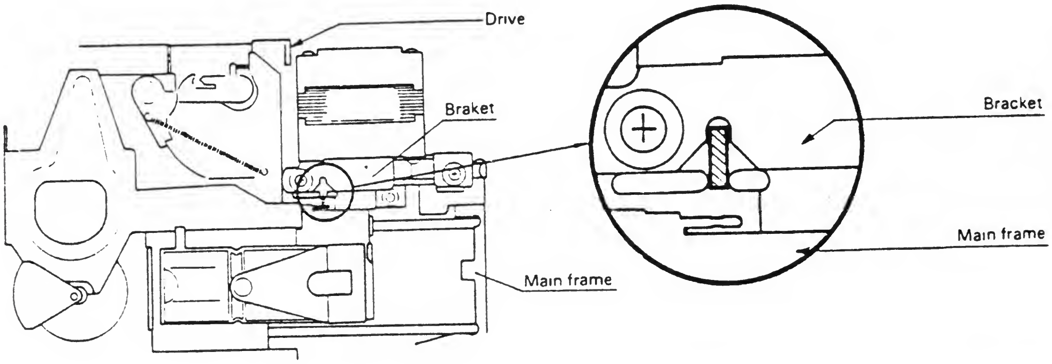


FIGURE 6-12. OFF-TRACK ADJUSTMENT

NOTE: If the off-track waveform has not been adjusted, repeat the above off-track waveform adjustment procedures as well as the adjustment of the track 00 position. (Section 6.2.3)

3. Secure the stepper motor clamping screws. Move the head from track 00 to track 34 and from track 39 to track 34, and check the off-track again.

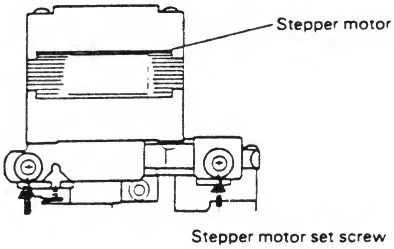


FIGURE 6-13. STEPPER MOTOR UNIT ASSEMBLY

Azimuth Check (Side 0)

The lower head azimuth cannot be adjusted; however, check the head for damage by performing the following procedures:

1. Make sure that the off-track adjustment for the lower head has been completed.
2. Insert the CE disk into a drive to activate the drive motor.
3. Press the CURRENT TRACK push button on the FMTC to position the head at track 34.
4. Observe the waveforms on the oscilloscope, and make sure that the ratios of B to C and C to B are 1.0 to 0.8. (Figure 6-14)

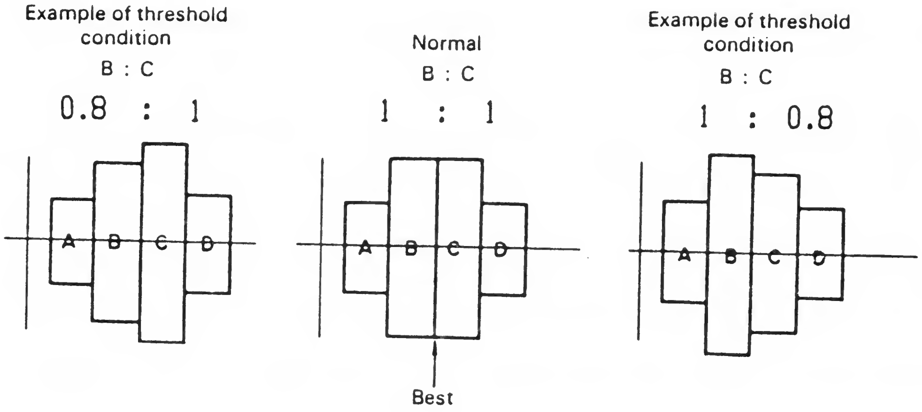

Example of threshold condition
B : C
0.8 : 1
Normal
B : C
1 : 1
Example of threshold condition
B : C
1 : 0.8
A
B
C
D
Best

FIGURE 6-14. AZIMUTH WAVEFORM (SIDE 0)

WARNING

The head carriage must be replaced if the ratio of B to C or C to B is less than 0.8.

Index Timing Adjustment (Side 0)

1. Make sure that the off-track adjustment for the lower head has been completed.
2. Insert the CE disk into the drive to activate the drive motor.
3. Press the CURRENT TRACK push button on the FMTC to position the head at track 34.
4. Observe that the index waveform on the oscilloscope is as shown in Figure 6-15.

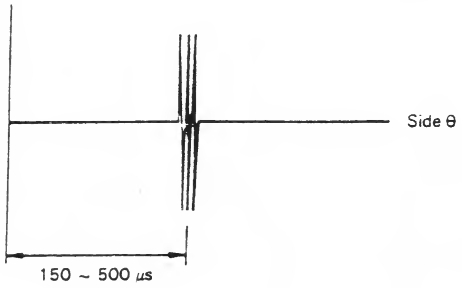


FIGURE 6-15. INDEX BURST WAVEFORM (SIDE 0)

5. If the index signal is incorrect, loosen the index detector securing screw by using a Phillips screwdriver until the signal is in the 150 - 500 us range. (Figure 6-16)

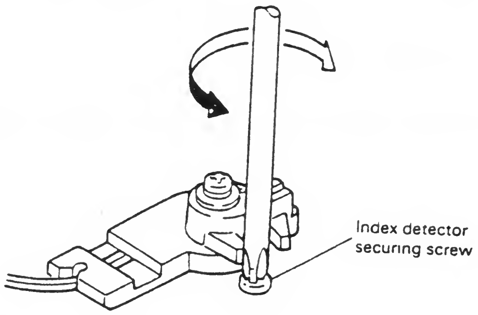


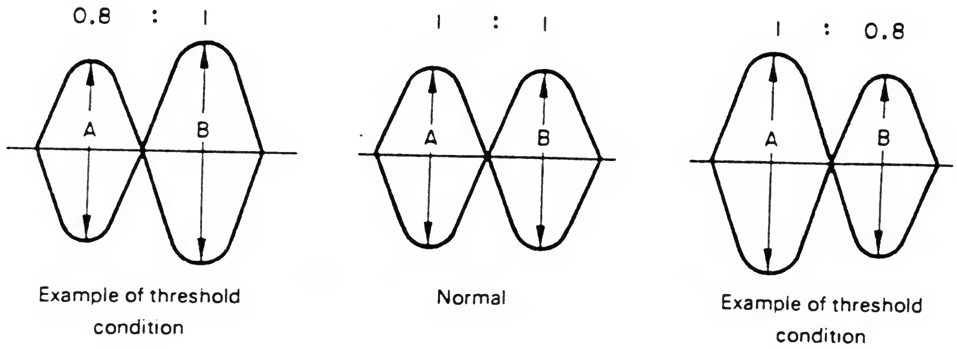
FIGURE 6-16. INDEX ADJUSTMENT POINT LOCATION

6. After completion of the adjustment, tighten the index detector clamping screw (torque to maximum 4.0 Kg/cm), and apply adhesive (screw lock green) over the clamping screw and its circumference.

6.2.2.2 Side 1 Adjustment

1. Set the SIDE switch of the FMTC to SIDE 1.
2. Turn the FMTC power switch on.
3. Insert the CE disk into the drive to activate the disk drive motor.
4. Press the CURRENT TRACK pushbutton on the FMTC, and check the off-track, azimuth, and index timing waveforms (Figure 6-19) when the head is moved in the following directions:
   Track 00 ------> Track 34
   Track 39 ------> Track 34

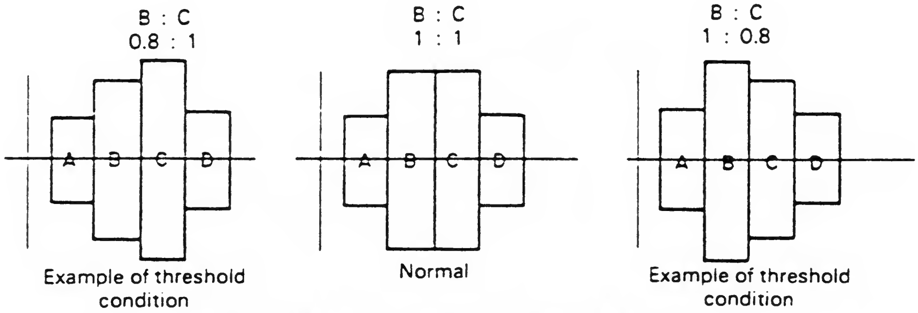
Off-Track Waveform 20 ms/DIV


0.8 : 1
A
B
Example of threshold condition
1 : 1
A
B
Normal
1 : 0.8
A
B
Example of threshold condition

Ratio of B against C or C against B should be 1 to 0.8.

FIGURE 6-17. OFF-TRACK WAVEFORM (SIDE 1)

Azimuth Waveform 200 ms/DIV


B : C
0.8 : 1
A
B
C
D
Example of threshold condition
B : C
1 : 1
A
B
C
D
Normal
B : C
1 : 0.8
A
B
C
D
Example of threshold condition

Ratio of B against C or C against B should be 1 to 0.8.

FIGURE 6-18. AZIMUTH WAVEFORM (SIDE 1)

Index Timing Waveform

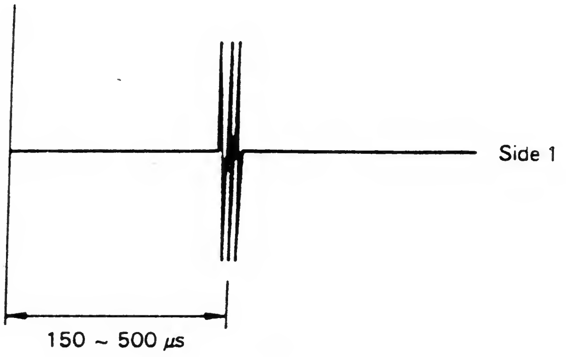


FIGURE 6-19. INDEX BURST WAVEFORM (SIDE 1)

If the off-track, azimuth and index timing waveforms do not meet specifications, adjust them as follows:

1. Loosen the upper head carriage set screws. (Figure 6-20)

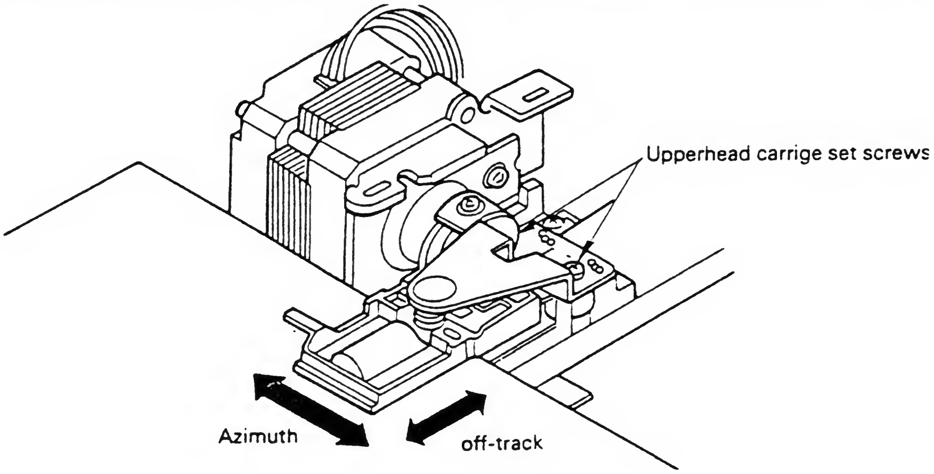


FIGURE 6-20. UPPER HEAD ADJUSTMENT

2. Manually adjust the upper head carriage (forward/backward and right/left) until the adjustments are as described above.

3. Tighten the upper head carriage set screws (torque to maximum 4 Kg/cm), and verify the off-track, azimuth, and index timing for side 1.

6.2.3 Track 00 Sensor Adjustment

1. Perform the off-track adjustment as described in Section
2. Connect the oscilloscope to TP3 on the main board and GND, and move the head to track 2.
3. Move the head to track 1, and check for a high-to-low inversion midway between tracks, as diagrammed in Figure 6-21.
4. Insert a Phillips screwdriver in the round hole on the control board. To adjust the track 00 sensor insert a flat-blade screwdriver in the oval hole on the board, positioning the sensor screw in the triangular adjustment area on the sensor.
5. Turn the Phillips screwdriver to loosen the adjusting screw, then adjust the sensor position with the flat-blade screwdriver (Figure 6-22) until the signal inversion occurs between tracks 2 and 1.
6. Tighten the screws after adjustment.

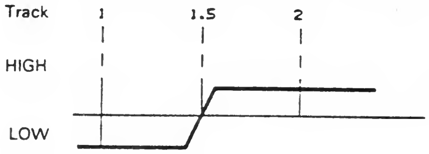


FIGURE 6-21. TRACK 00 SENSOR WAVEFORM

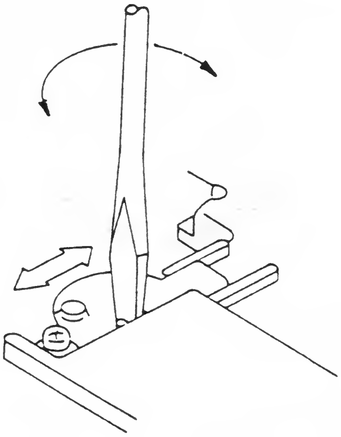


FIGURE 6-22. TRACK 00 SENSOR ADJUSTMENT POINT LOCATION

6.3 SD-581L FLOPPY DISK DRIVE ADJUSTMENT

The following adjustments using the listed devices and tools are required.

TABLE 6-4. SD-581L FLOPPY DISK DRIVE ADJUSTMENT EQUIPMENT

ADJUSTMENT	DEVICE	TOOL.ECT.
Head load lever gap adjustment	FDD controller (FMTC-II, FAT, etc.)	* Adjusting disk Dymek CE DK 502-11 D * Disk * Phillips (+) screwdriver #1 * (-) blade screwdriver #1 * (-) blade adjusting screwdriver #2 * Torque screwdriver * Feeler gauge * Adhesive * Screw locking agent #1406
Off-track adjustment		
Index position adjustment	Oscilloscope (Two phenomena)	
Track 00 sensor position adjustment		

* FMTC-II and FAT are both the FDD controlling and measuring device recommened by EPSON; other devices having the same function may be used. For measurement of the head output by FAT, use a probe directly connected to 1M ohm or an FET probe. For other purposes, ordinary probes can be used.

6.3.1 Positions and Funtions of Test Points

The SD-581L has 11 test points on the control circuit for observation of signal waveforms used in adjustment and inspection.

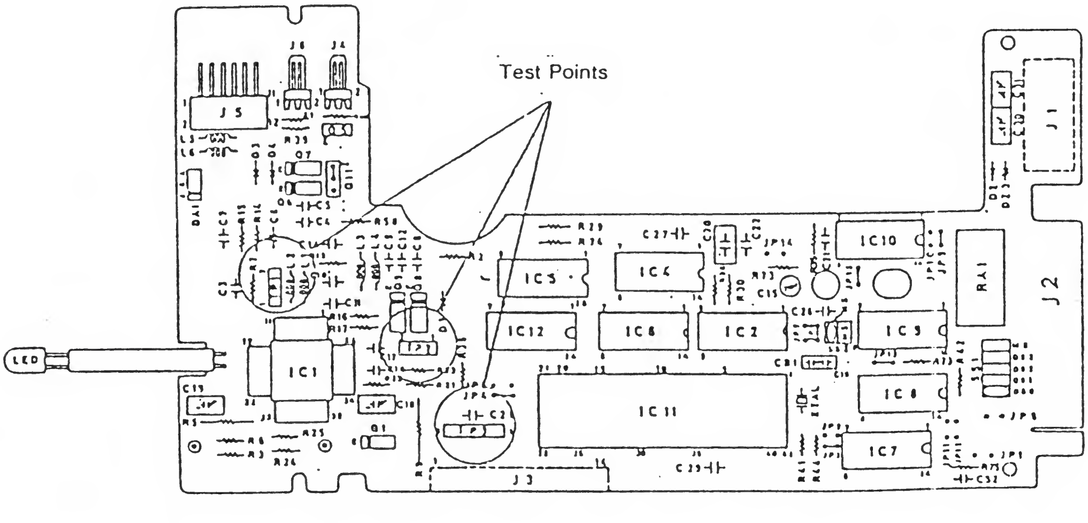
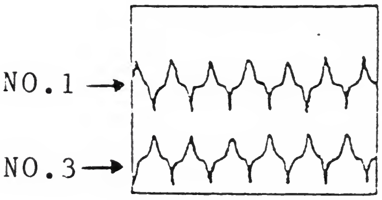
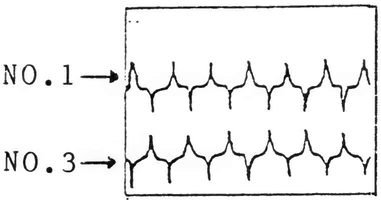
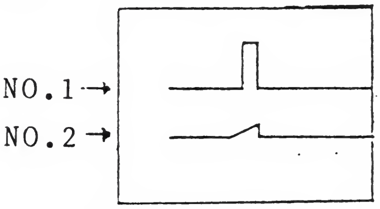
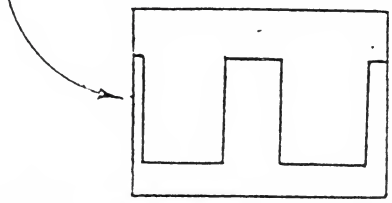


FIGURE 6-23. SD-581L CONTROL BOARD TEST POINT LOCATIONS

The function of the test points are as follows:

TABLE 6-5. SD-581L CONTROL BOARD TEST POINTS

TP NO.	PIN NO.	USE
TP1	Pins 1 and 3	These are the test points for observation of read amp (CX20185) output. Differential waveform with 180 phase difference appears at pins 1 and 3.
	Pin 2	This is the 0V (GND) line of the analog signal system, which is the reference point for observation of signal waveforms TP1 and TP2. * These are used for the checking of various performance characteristics of the read/write head and the adjustment of the haed access mechanism (off-track, azimuth etc).
		
TP2	Pins 1 and 3	These are the test points for observation of differential amp output. As with TP1, differential waveform with 180 phase difference appears at pins 1 and 3.
	Pin 2	Like TP1-2, this is the 0V (GND) line of the analog signal system. * These are used for the checking of the total function of the read/write head and amp system using FAT or the like.
		
TP3	Pins 1 and 2 	These are the test points for observation of the index detection output. Signal of opposite level appear at pins 1 and 2. They are used as trigger signal for the checking of the period of disk rotation and the observation of off-track and azimuth signals.
	Pin 3 (or J3-7)	This is the test point for observation of track 00 sensor output.
	Pin 4	This is the test point for observation of the Drive Select signal.
	Pin 5	This is the 0V (GND) line of the digital signal system, which is the reference point for observation of signal waveformes of TP3. * The index detection output is generally taken from the INDEX terminal of FMTC-II.
		

6.3.1 Head Load Lever Gap Adjustment

1. Set and turn the disk, and perform a head loading.
2. Insert the feeler gauge in the gap between the head load lever and the upper carriage arm.
3. Move the head roller arm back and forth by turning the (-) blade screwdriver clockwise and counterclockwise in the adjustment groove of the head load lever and make a gap adjustment at the head load cam face.
   (Gap : 0.2 to 0.6 mm)
4. After the gap adjustment, tighten the haed load lever setscrews using the Phillips (+) screwdriver.
   (Screw tightening torque : about 4.0 Kg cm)
5. Apply Screw Locking Agent #1406 for more than 1/4 of the contact circumference between the setscrews and the head load lever.

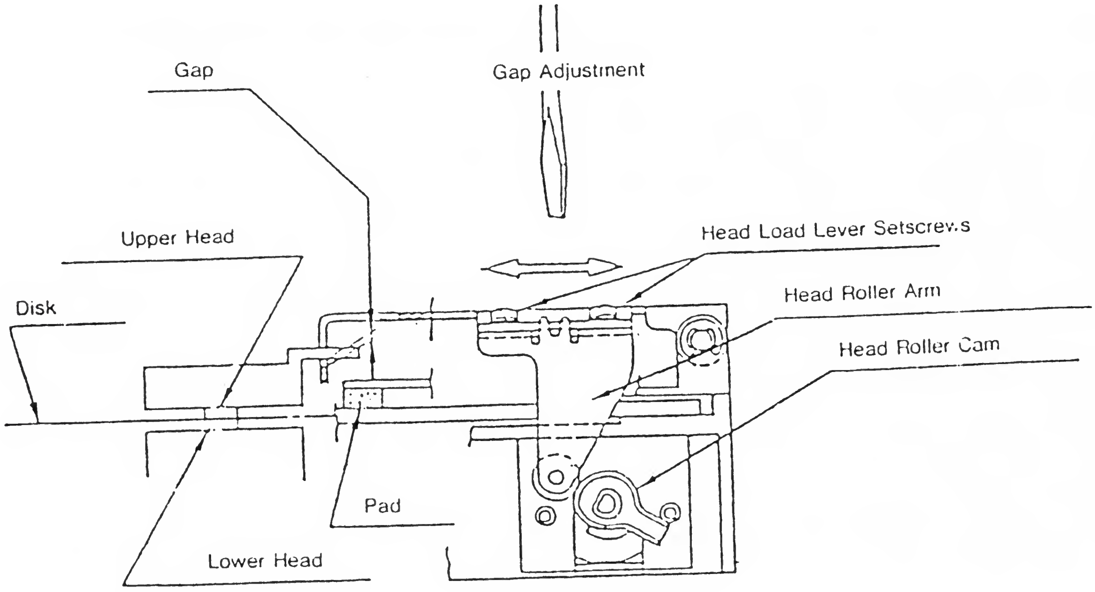


FIGURE 6-24. HEAD LOAD LEVER GAP ADJUSTMENT

6.3.2 Off-Track Adjustment

1. Connect CH1 of the oscilloscope with TP1-1, CH2 with TP1-3 and the external trigger with the INDEX output terminal of FMTC-II, respectively. (Trigger is to be in "-" direction.)
2. Set the signal conditions of the oscilloscope as follows:

SWITCH	CH1 and 2
AC-GND-DC	AC
VERT MODE	ADD
INVERT	ON
VOLTS/DIV	50 mV
TIME/DIV	20 mS

3. Turn the spindle motor.
4. Insert the CE disk and load the head.
5. Move the head from track 00 to track 68 manually.
   This operation must be repeated from track 00 when the head has overrun track 68.
6. Observe the waveform on the oscilloscope.
7. Insert the (-) blade screwdriver in the adjustment groove of the step motor bracket and make an adjustment so that the ratio of A to B (small/large) in Figure 6-25 becomes more than 0.7.
   Figure 6-26 shows the off-track measured with a Dymek CE disk.
8. Tighten the motor bracket setscrews (a) and (b) when the ratio of A to B (small/large) of the waveform in Figure 6-25 is 0.7 or greater.
   CPSP M2.5 x 6 -------- a, b
   (Screw tightening torque : about 6.0 Kg cm)
9. Apply Screw Locking Agent #1406 for more than 1/4 of the contact circumference between the setscrews and the bracket.

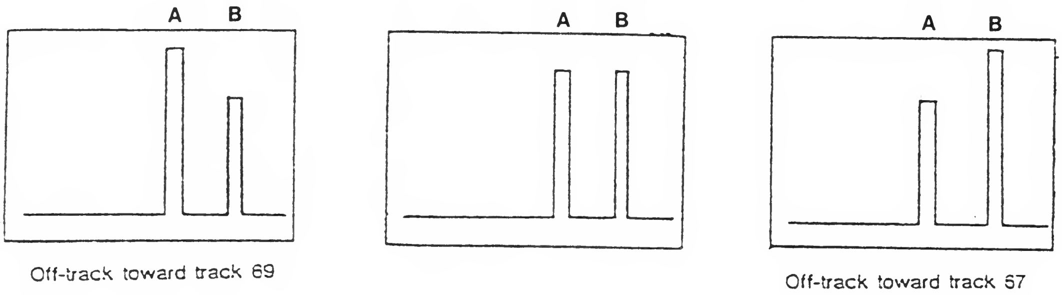


FIGURE 6-25. TP1-1 AND TP1-3 OUTPUT WAVEFORMS

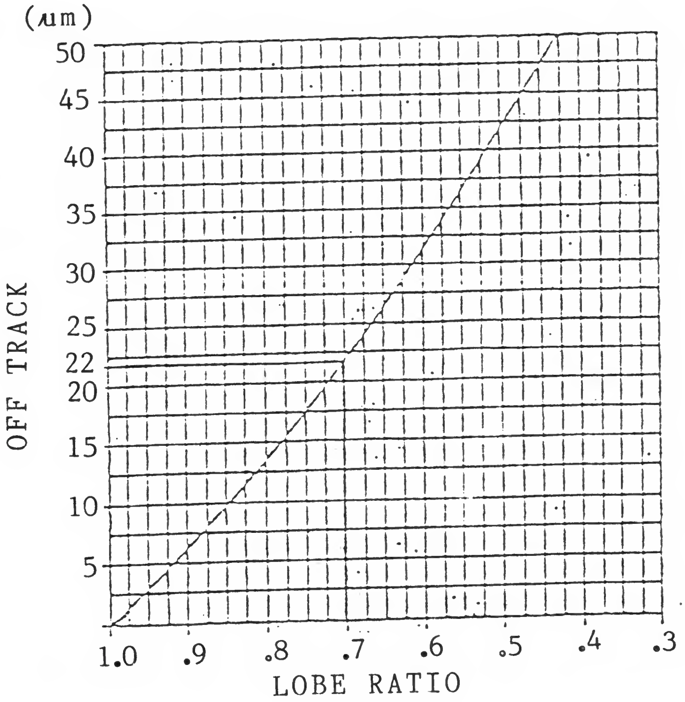


FIGURE 6-26. OFF TRACK

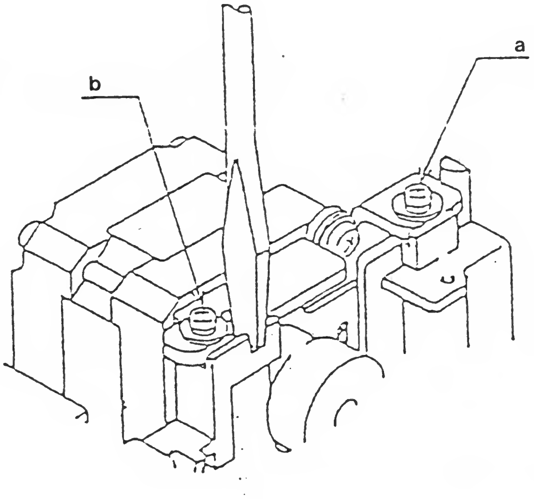


FIGURE 6-27. OFF-TRACK ADJUSTMENT

6.3.3 Index Position Adjustment

1. Connect CH1 of the ocsilloscope with TP1-1, CH2 with TP1-3 and the external trigger with the INDEX output terminal of FMTC-II, respectively.
2. Set the signal conditions of the oscilloscope as follows:
   (Trigger is to be in "-" direction.)

SWITCH	CH1		CH2
AC-GND-DC	AC		AC
VERT MODE		ADD	
INVERT	-		ON
VOLTS/DIV	50 mV		50 mV
TIME/DIV		50 us	

3. Turn the spindle motor.
4. Insert the CE disk and perform a head loading.
5. Move the head to track 68.
6. Observe the waveform on the oscilloscope.

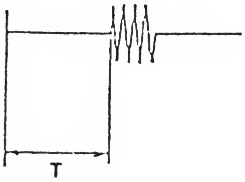


FIGURE 6-28. TP1-1 AND TP1-3 OUTPUT WAVEFORM

7. Loosen the index sensor setscrew (a) when the time T of the waveform in Figure 6-28 is not in the following range at SIDE 0:
   250 + 100 us (HIGH)
   300 + 300 us (NORM)
8. Insert the tip of the Phillips (+) screwdriver between the adjustment claws of the index sensor A and adjust the index position so that the time T comes within the following range both at SIDE 0 and SIDE 1:
   250 + 100 us (HIGH)
   300 + 300 us (NORM)

   Also, the time difference between SIDE 0 and SIDE 1 must be 130 us or less.
9. Tighten the index sensor A setscrew (a), taking care to keep the index position setting. (Screw tightening torque : about 2.5 Kg cm)
10. Apply Screw Locking Agent #1406 to the contact circumstance between the index sensor A setscrew (a) and the index sensor.

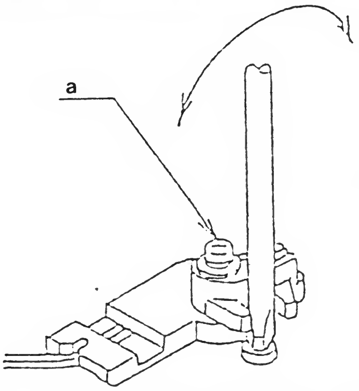


FIGURE 6-29. INDEX POSITION ADJUSTMENT

6.3.4 Track 00 Sensor Position Adjustment

1. Confirm track 68 by the off-track adjustment procedure. (Section 6.3.2)
2. Connect the lead wire of the oscilloscope or DC multimeter to the connector J3-7 on the main circuit board or to TP3-3 and GND.
3. Move the carriage to track 3.
4. Put the phillips (+) screwdriver to the 00 sensor adjustment screw (a) through the round hole in the main circuit board and the (-) blade screwdriver into the triangle hole of the track 00 sensor through the elliptical hole. (Refer to Figure 6-30)
5. Make a positional adjustment with the (-) blade screwdriver so that the signal level turns from "HIGH" to "LOW" when the carriage is moved from track 3 to track 2.
6. Tighten the screw (a) upon completion of the adjustment.

CPSP M2.5 x 6 ----- a
(Screw tightening torque : about 3.5 Kg cm)

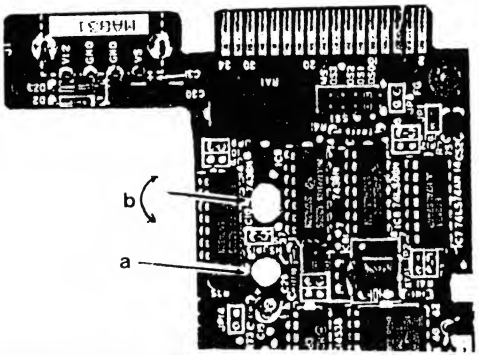


FIGURE 6-30. TRACK 00 SENSOR ADJUSTMENT

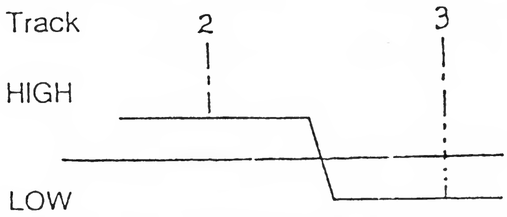


FIGURE 6-31. J3-7 OUTPUT WAVEFORM

6.4 HD-860 HARD DISK DRIVE ADJUSTMENT

This section explains the services that can be performed on HD-860 series without clean room facilities. HD-860 disk drives are manufactured in a clean environment to eliminate contaminations. Then it is strongly prohibited to disassemble or open HDA at unauthorized facilities. The assemblies that can be replaced by customers include the followings:

(1) Front Bezel
(2) PCB
(3) Mounting Frame
(4) Main Track Zero Sensor
(5) Carriage Lock Unit

CAUTION

Preventive maintenance is not required to maintain the drive operation status. However, when repaire or adjustment are needed, the following cautions must be observed.

(1) Great care must be paid so that the drive may not sustain severe shocks or vibrations. It is recommended that shock dampers such as rubber or cushions should be laid under the drive. HD-860 series are designed to withstand shocks up to 40G, which is equivalent to shocks when one corner of the drive is lifted 0.4 inch or 10 mm and dropped on the steel surface. If the drive suffers shocks more than 40G, heads and/or disks may get damaged and can't be repaired without data loss. However, if the rubber with 0.3 inch or 8 mm thick is laied, the shocks will be reduced to about 15G.
(2) Before the customer repairs the drive or replaces parts, make sure that powers of the drive are cut off completely and the power cable is disconnected.
(3) Don't lose or remove any screws or seals which are not designated in each section, otherwise HDA will lose air-tightness and be contaminated.
(4) Don't rotate the stepper or the spindle motor by hand, otherwise heads and/or disks will be damaged.
(5) In disconnecting cables, grip connectors and pull them straight forwardly. Don't pull cables, or cables will be open circuited.
(6) Tighten screws with the designated torque in each section. Adhesive bond can be used only in the designated areas.
(7) For cleaning the drive, use only dry soft textile. Avoid using water, organic solvent or cleanser.
(8) Servicemem must ground themselves with rist earth bands.

6.4.1 Mian Track Zero Sensor Adjustment

1. Note the original conditions of the DIP switch. (Figure 6-32)
2. Change the DIP switch as follows.
    1 -- ON
    2 -- OFF
    3 -- ON
    4 -- Don't change
3. Apply DC +5V and +12V to the drive.
4. Ensure that the LED starts lighting in 20 sec.
5. If 4 succeeded, go to 7. If 4 failed, go to 6.
6. With loosing mounting screws of the main track zero sensor, adjust the sensor vertically as shown in Figure 6-30 so that the LED begins to light and then lock the mounting screws with 1 Kg-cm or 0.9 pound-inch. Remember that the range of sensor adjustment must be within +0.04 inch or +1 mm vertically. Adjustment of more than 0.063 inch or 1.6 mm will cause the shift of the track zero position on disks.
7. Turn off No.1 DIP switch, then the spindle motor will stop after heads are moved to the head landing zone.
8. Power off the drive.
9. Return all the DIP switch positions as noted in (1).

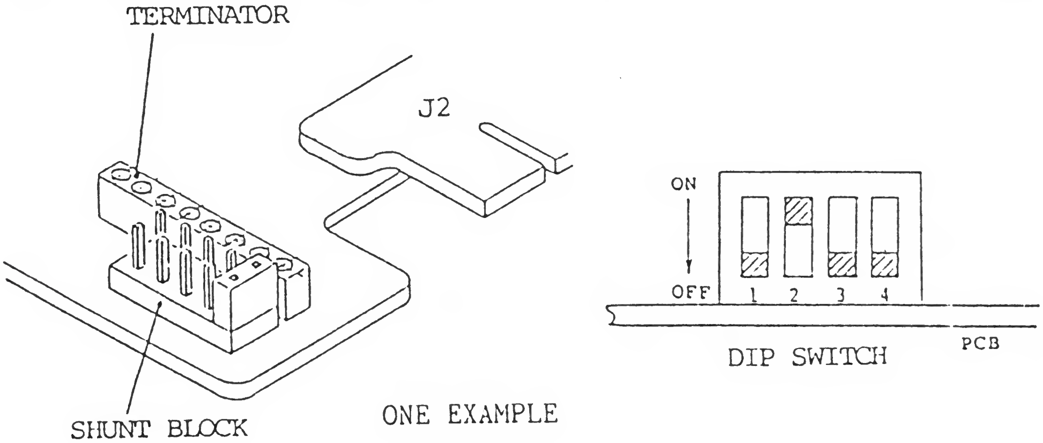


FIGURE 6-32. DIP SWITCH SETTINGS

6.4.2 Carriage Lock Adjustment

1. Connect the carriage lock cable (blue) to the PCB.
2. Connect the power cable.

CAUTION

Following steps 3 through 4 must be performed within 40 sec. If 40 sec elapses, the solenoid will be inactivated. In this case, power off the drive and retry from step 3 again or push and hold the pawl by hand as Figure 6-33 and go to step 4.

3. Power on the drive and push the top of the solenoid so that the solenoid pulls the pawl and release the gear wheel of the stepper.
4. Insert the gauge between the pawl and the gear wheel and adjust the carriage lock unit so that there is a clearance of 0.008 inch to 0.015 inch or 0.2 mm to 0.4 mm.

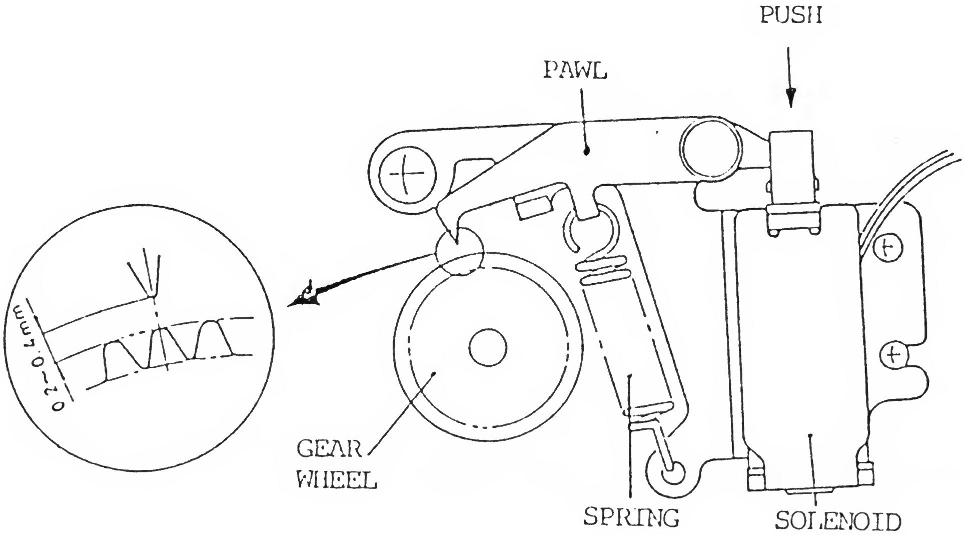


FIGURE 6-33. CARRIAGE LOCK ADJUSTMENT

6.5 ADJUSTMENT AND CONFIRMATION

After replacement of service parts, the following items need to be adjusted and confirmed. For these adjustments, an extension cable is used to take out sample signals. (The pin arrangement of the cable is the same as that on J1 of the main PCB).

1. Adjustment of the index burst position.
2. Confirmation of the reproduced output.
3. Adjustment of asymmetry.
4. Adjustment of the erase off delay time.
5. Adjustment of the track position.
6. Adjustment of the track 00 position.
7. Adjustment of the 0-1 head clearance. (Only with solenoid drive)
8. Confirmation of the WRITE PROTECT signal.
9. Confirmation of the LED indicator illumination.
10. Confirmation of the modulation.
11. Confirmation of the clamp mechanism action.

6.5.1 Adjustment of Index Burst Position

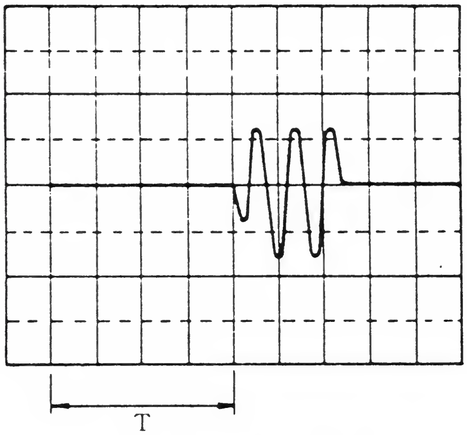


FIGURE 6-34. ADJUSTMENT OF INDEX BURST POSITION

a. Activate the MDD.

b. Load an alignment disk and step it to track 34.

c. Take measurements with an oscilloscope. The connections are as follows:
CH1 200mV AC CHK1—2
CH2 200mV AC INV CHK1—3
MODE ADD
TIME BASE 50 μsec
TRIGGER EXT NORM NEG CHK—2
(INDEX signal terminal)

d. Make sure that T, from the beginnig of the sweep to that of the index burst, is identical to the value given below ; if adjustment is necessary, move the phototransistor holder. Start with side 1 first.

Adjustment	Track 34	Both sides	200 ±50 μsec

6.5.2 Confirmation of Reproduced Output

a.Activate the MDD.
b.Load a normal disk.
c.Connect an oscilloscope as follows:
CH1 100 mV AC CHK1—2
CH2 100 mV AC INV CHK1—3
MODE ADD
TIME BASE 20 msec
TRIGGER EXT NORM NEG CHK2 (INDEX terminal)
d.Write 1F on track 00 and 2F on track 39 of both sides. Compare the output of both sides and confirm that the difference is within the following.

Track 39	0.40 V min.	Track 00	3.5V max.

Note 4: Track 00 ············ output value of side 1 or 0, whichever is larger
Track 39 ··· ······· output value of side 1 or 0, whichever is smaller

6.5.3 Adjustment of Asymmetry

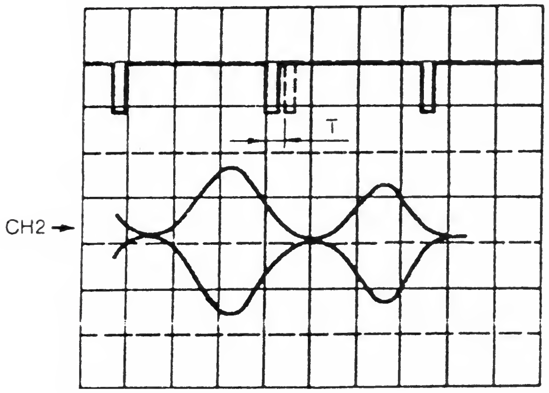


FIGURE 6-35. ADJUSTMENT OF ASYMMETRY

a.Activate the MDD.
b.Load a normal disk.
c.Connect an oscilloscope.
CH1 2V AC CHK 1—2
CH2 200 mV AC INV CHK1—3
MODE ADD
TIME BASE 1 μsec
TRIGGER INT CH1 NORM NEG
d.Write 1F on track 39 and adjust the trigger so that the wave forms of CH2 will be a "cat's eye."
e. Adjust VR 1 so that T will be within ±600 nsec at track 00 and track 39 on both sides.

6.5.4 Adjustment of Erase Off Delay

a.Activate the MDD.
b.Load a normal disk.
c.Connect an oscilloscope as follows:
CH1 2V DC CHK4 (WRITE GATE terminal)
CH2 2V DC CHK3 (ERASE terminal)
MODE CHOP
TIME BASE 0.2 msec
TRIGGER INT CH1 POS
d.Adjust VR2 so that the erase current is off within 972 μsec ± 20 μsec from the closing of the WRITE GATE.

6.5.5 Adjustment of Track Position

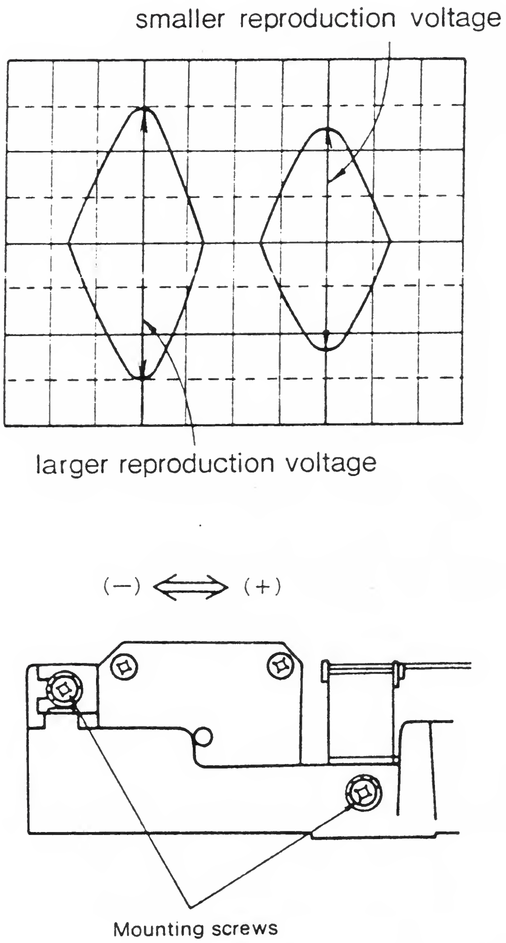


FIGURE 6-36. ADJUSTMENT OF TRACK POSITION

a.Activate the MDD.
b.Loosen the screws for the step motor and insert an alignment disk and step it to track 16 .
c.Take measurements with an oscilloscope. The connections are as follows :
CH1 500mV AC CHK1—2
CH2 500mV AC INV CHK1—3
MODE ADD
TIME BASE 20 msec
TRIGGER EXT NORM NEG CHK2
(INDEX signal terminal)
d.Select side 0 and 1 alternately, monitor the wave forms reproduced on a screen and adjust the output ratios or both sides so that they are within the following limits:
In case of MDD 531, 80% or less.

$$\text{Output ratio} = \frac{\text{smaller regenereted voltage}}{\text{larger regenereted voltage}} \times 100$$

e.Tighten mounting screws A and B.

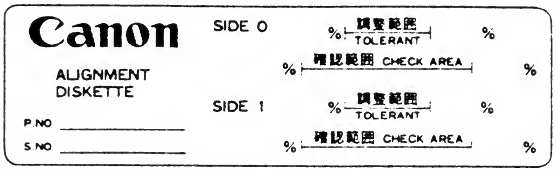


FIGURE 6-37. RANGE OF ALIGNMENT DISK ADJUSTMENT AND CONFIRMATION

f. Make the head step from track 15 to track 16 and track 17 to track 16 and confirm in both cases that the output ratios on both sides are within the following limits.
   For the MDD531, within 70 %.
   If the output ratio is out of the range, make adjustments again.

Define + or − in relation to the wave forms on the oscilloscope screen.
The output ratio is calculated by the equation shown in part d. of Section 6.5.5.
Adjustment of the track position : judge the polarity from the relative sizes of bursts A and B.

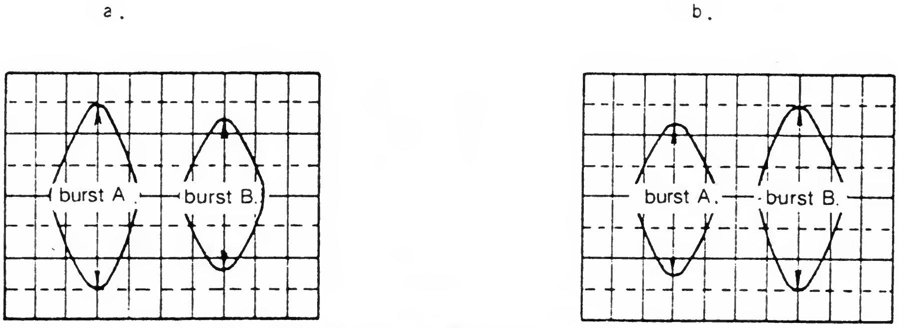


FIGURE 6-38. ADJUSTMENT OF TRACK POSITION

negative, when burst A > burst B

positive, when burst A< burst B

6.5.6 Adjustment of Track 00 Position

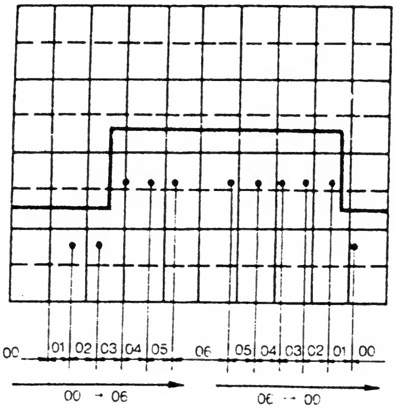


FIGURE 6-39. ADJUSTMENT OF TRACK 00 POSITION

a. Activate the MDD.
b. Load a normal disk.
c. Step the head between tracks 00 and 06 alternately.
d. Take measurements with an oscilloscope.
   The connections are as follows:
   CH1 5V DC STEP signal terminal
   CH2 2V DC INV CHK1–3
   MODE ADD
   TIME BASE 5 msec
   TRIGGER INT CH2 NORM POS

e.Confirm that the switching position is track 03 in the direction of track 00 to track 06 and track 01 in the direction of track 06 to track 00. If necessary, make adjustments by loosening the mounting screws of the track 00 switch assembly.

6.5.7 Adjustment of 0-1 Head Space

(for the MDD with optional head load solenoid)

Adjust the head space between side 0 and side 1 when clamped without a disk. **NOTE 1:**

a. Remove the main PCB and insert a clearance gauge from the side of the head. Loosen the screws (2 pcs.) for the head load arm by a quarter of a revolution.

b. Move the head load arm and adjust the head space so that the clearance gauge has a little freedom. At the same time, adjust the main arm so that it will be parallel with the head load arm and tighten the mounting screws.

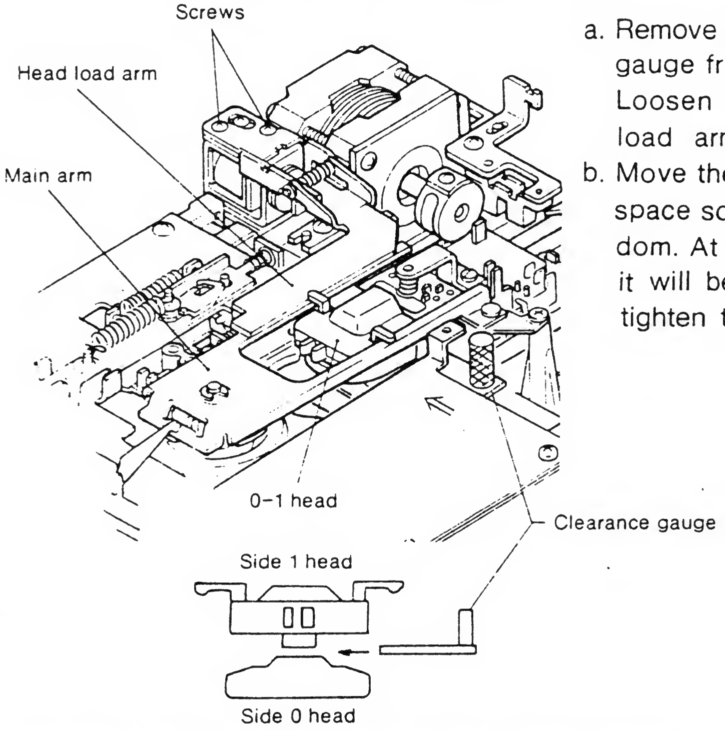


FIGURE 6-40. ADJUSTMENT OF 0-1 HEAD SPACE

Note 1 : To attain a clamped state without a disk.

a. Push ① in the direction shown by an arrow in the figure below.

b. Cancel the clamped state by pushing the button after adjustment.

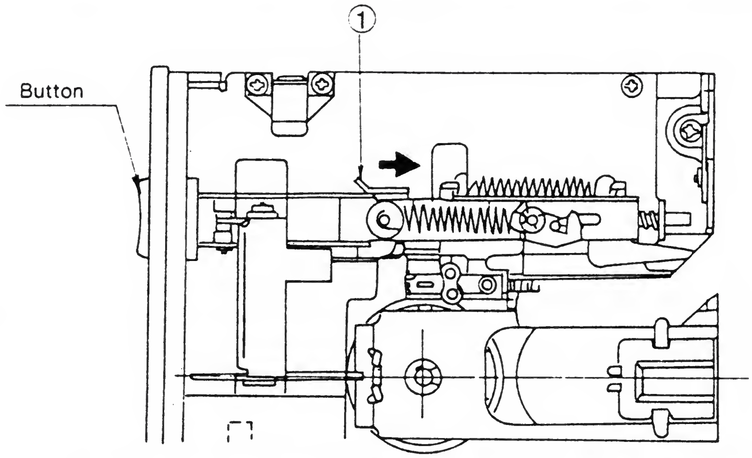


FIGURE 6-41. ADJUSTMENT OF 0-1 HEAD SPACE

6.5.8 Confirmation of WRITE PROTECT Signal

a. Activate the MDD.
b. Insert a disk not write protected and confirm with an oscilloscope that pin J1—28 on the main PCB assembly changes.
c. Insert a write protected disk and confirm with oscilloscope that pin J1—28 on the main PCB assembly does not change.

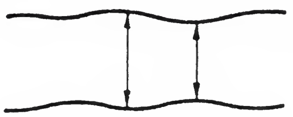
6.5.9 Confirmation of LED Operation

a. Activate the MDD and confirm that the LED indicators come on in compliance with each LED lighting mode.

6.5.10 Confirmation of Modulation

a. Load a normal disk and write 2F ; confirm that the amplitude of the envelope has the following value.
b. Connect an oscilloscope as in Section 6.5.2.

Track 00, 39	Both sides	10% max.

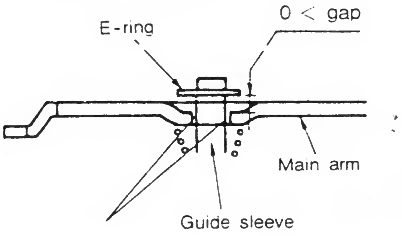


$$\text{Modulation} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \times 100\%$$

FIGURE 6-42. CONFIRMATION OF MODULATION

6.5.11 Confirmation of Clamp Mechanism

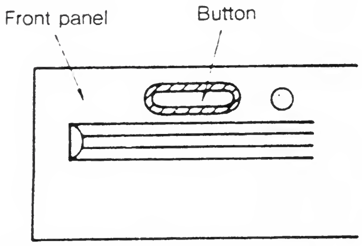
1) Main arm gap



a. When the clamped state and unclamped state, the button should not touch the front panel.
b. When the clamped state is made without a disk, there should be space between the bottom of the E-ring and the concave section of the main arm.

FIGURE 6-43. CONFIRMATION OF CLAMP MECHANISM

2) Button gap



a. When the clamped state and unclamped state, the button should not touch the front panel.

FIGURE 6-44. CONFIRMATION OF CLAMP MECHANISM

CHAPTER

7

DIAGRAMS AND REFERENCE MATERIALS

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7.1 DIP SW SETTING

Tables 7-1 and 7-2 show the settings of DIP switches 1 and 2, respectively.

TABLE 7-1. DIP SW1 SETTINGS

	1	2	4	5	6	7	8
Floppy drive A:							
360KB	ON						
1.2MB	OFF						
Coprocessor:							
Installed		OFF					
Not installed		ON					
Internal parallel interface:							
Primary			OFF				
Secondary			ON				
Monitor type:							
Disable internal video				ON	ON		
Color (40 X 25)				OFF	ON		
Color (80 X 25)				ON	OFF		
Monochrome				OFF	OFF		
Number of floppy disk drives:							
One						ON	ON
Two						OFF	ON

TABLE 7-2. DIP SW2 SETTINGS

	5	7	8
Parity checking:			
Enable	OFF		
Disable	ON		
Internal serial interface:			
Primary		OFF	
Secondary		ON	
Internal serial interface:			
Enable			OFF
Disable			ON

7.2 JUMPER SETTING

J1 and J2

J1	J2	FUNCTION	FACTORY SETTING
1-2 Short	1-2 Short	Invalid of the DACKO of 8237	-

J1	J2	FUNCTION	FACTORY SETTING
3-2 Short	3-2 Short	Valid of the DACKO of 8237	on

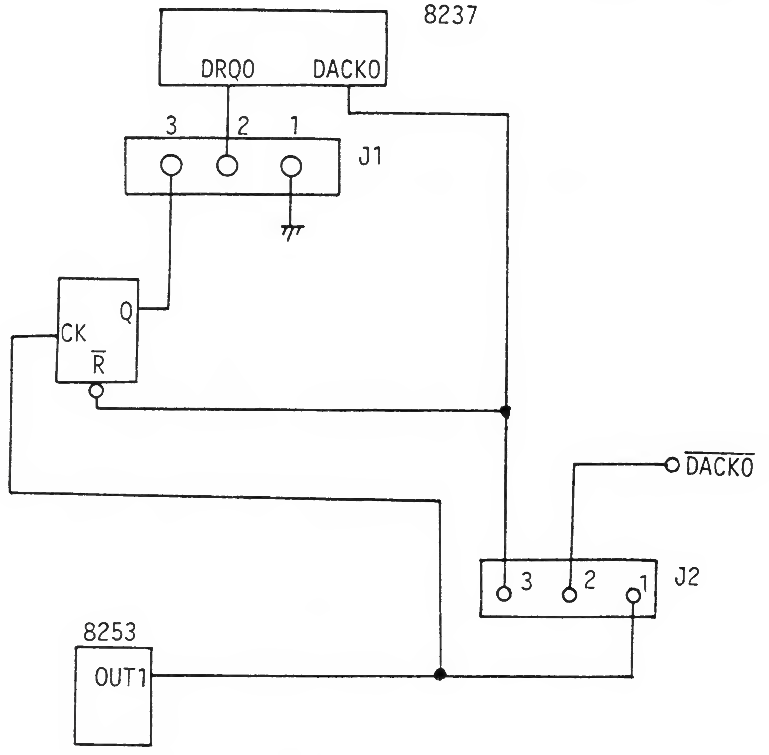

FIGURE 7-1. JUMPER LOCATION

7.3 PIN ASSIGNMENT OF CONNECTORS (Figures 7-2 through 7-15)

The interconnection of the main CPU unit, floppy disk drive, and monitor is summarized in Table 7-3. Pin assignment for each connector is detailed in Tables 7-4 through 7-18.

TABLE 7-3. CONNECTOR SUMMARY

CONNECTOR	TYPE	DESCRIPTION	REFERENCE
CN1	MOREX,5271-07A,5275-09A	To Power Supply Unit	Table 7-4
CN2	HIROSE,PCN10A-64P-2.54DS	To Mother Board (MCY-MT)	7-5
CN3	HONDA,GMM-X25UGDFDB1	Printer I/F Port	7-6
CN4	HONDA,GMM-X25UGDMDB1	RS-232C Port	7-7
CN5	HONDA,GMM-X9UGDFDB1	Monitor Port	7-8,9
CN6	HOSHIDENKI,JPJ-2545-01-510	Composit Video Port	7-10
CN8	HOSHIDENKI,TCS5040-18-1011	Keyboard Port	7-11
CN9,CN10	DDK,FRC5-C34S53T-OS(D20)	FDD Control Port	7-12
CN11	ELCO,00-8283-0512-00-000	To Power SW and LED	7-13
CN12	ELCO,00-8283-0212-00-0000	To Speaker	7-14
CN13	JAE,IL-2P-S3FP2	To Battery	7-15
CN14	HIROSE,PCN10-48S-2.54DSA	RAM Card I/F Board	7-16
Slot #1-#4	DDK,226D-10031L2-2320	Option Card Ports	7-17
Slot #5	DDK,226D-10031L2-2320	Option Card Port	7-18

Connector CN1

Use: To power supply unit
Type: MOREX, 5271-07A, 5275-09A

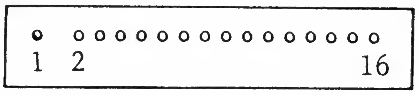

FIGURE 7-2. CN1 PIN LOCATIONS

TABLE 7-4. CN1 PIN ASSIGNMENT

PIN No.	SIGNAL	DIRECTION	DESCRIPTION
1	GP	-	Ground
-	-	-	N/C
2	+12	-	+12 V
3	-12	-	-12V
4	$\overline{\text{PWDN}}$	I	Power down
5	PWON	O	Power on
6	-5 V	-	-5 V
7	NOSW + 5	-	Unswitched +5 V
8	+5 V	-	+5 V
9	+5 V	-	+5 V
10	+5 V	-	+5 V
11	+5 V	-	+5 V
12	GL	-	Ground
13	GL	-	Ground
14	GL	-	Ground
15	GL	-	Ground
16	GL	-	Ground

NOTE: Signal direction is as viewed from the MCY board.

Connector CN2

Use : To mother board (MCY-MT)
Type: HIROSE, PCN10A-64P-2.54DS

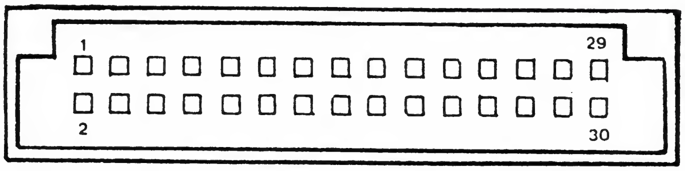

FIGURE 7-3. CN2 PIN LOCATIONS

TABLE 7-5. CN2 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
A1	$\overline{\text{IOCHCK}}$	I	I/O Channel Check
A2	D7	I/O	Data Bit 7
A3	D6	I/O	Data Bit 6
A4	D5	I/O	Data Bit 5
A5	D4	I/O	Data Bit 6
A6	D3	I/O	Data Bit 4
A7	D2	I/O	Data Bit 3
A8	D1	I/O	Data Bit 2
A9	D0	I/O	Data Bit 1
A10	IOCHRDY	I	Data Bit 0
A11	AEN	O	I/O Channel Ready
A12	A19	O	Address Latch Enable
A13	A18	O	Address Bit 19
A14	A17	O	Address Bit 18
A15	A16	O	Address Bit 17
A16	A15	O	Address Bit 16
A17	A14	O	Address Bit 15
A18	A13	O	Address Bit 14
A19	A12	O	Address Bit 13
A20	A11	O	Address Bit 12
A21	A10	O	Address Bit 11
A22	A9	O	Address Bit 10
A23	A8	O	Address Bit 9
A24	A7	O	Address Bit 8
A25	A6	O	Address Bit 7

A26	A5	O	Address Bit 6	
A27	A4	O	Address Bit 5	
A28	A3	O	Address Bit 4	
A29	A2	O	Address Bit 3	
A30	A1	O	Address Bit 1	
A31	A0	O	Address Bit 2	
B1	GND	-	Ground	
B2	RESETDRV	O	Reset Driver	
B3	+5 V	-	+5 V	
B4	IRQ2	I	Interrupt Request 2	
B5	-5VDC	-	-5 V	
B6	DRQ2	I	DMA Request 2	
B7	-12 V	-	-12 V	
B8	**(RESERVED)**	-	**Not used**	B
B9	+12 V	-	+12 V	
B10	GND	-	Ground	
B11	$\overline{\text{MEMW}}$	O	Memory Write Command	
B12	$\overline{\text{MEMR}}$	O	Memory Read Command	
B13	$\overline{\text{IOW}}$	O	I/O Write Command	
B14	$\overline{\text{IOR}}$	O	I/O Read Command	
B15	$\overline{\text{DACK3}}$	O	DMA Acknowledge 3	
B16	DRQ3	I	DMA Request 3	
B17	$\overline{\text{DACK1}}$	O	DMA Acknowledge 1	
B18	DRQ1	I	DMA Request 1	
B19	$\overline{\text{DACK0}}$	O	DMA Acknowledge 0	
B20	CLOCK	O	Clock (4.77 MHz duty 33%)	
B21	IRQ7	I	Interrupt Request 7	
B22	IRQ6	I	Interrupt Request 6	
B23	IRQ5	I	Interrupt Request 5	
B24	IRQ4	I	Interrupt Request 4	
B25	IRQ3	I	Interrupt Request 3	
B26	$\overline{\text{DACK2}}$	O	DMA acknowledge 2	
B27	T/C	O	Terminal Count	
B28	ALE	O	Address Latch Enable	
B29	+5 V	-	+5 V	
B30	OSC	O	Oscillator (14.31818 MHz)	
B31	GND	-	Ground	

NOTE: Signal direction is as viewed from the MCY board.

Connector CN3

Use : Printer I/F port
Type: HONDA, GMM-X25UGDFDB1

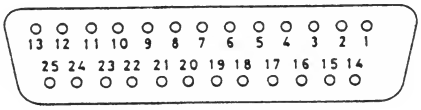

FIGURE 7-4. CN3 PIN LOCATIONS

TABLE 7-6. CN3 PIN ASSIGNMENT (Parallel Printer)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	$\overline{\text{STROBE}}$	O	Strobe
2	DATA0	O	Data Bit 0
3	DATA1	O	Data Bit 1
4	DATA2	O	Data Bit 2
5	DATA3	O	Data Bit 3
6	DATA4	O	Data Bit 4
7	DATA5	O	Data Bit 5
8	DATA6	O	Data Bit 6
9	DATA7	O	Data Bit 7
10	$\overline{\text{ACK}}$	I	Acknowledge
11	BUSY	I	Busy
12	PE	I	Paper Empty
13	SLCT	I	Select
14	$\overline{\text{AUTOLFXT}}$	O	Auto Line Feed XT
15	$\overline{\text{ERROR}}$	I	Error
16	$\overline{\text{INIT}}$	O	Initialize
17	$\overline{\text{SLCTIN}}$	O	Select In
18-25	GND	-	Signal Ground

NOTE: Signal direction is as viewed from the MCY board.

Connector CN4

Use : RS-232C Port
Type: HONDA, GMM-X25UGDMDB1

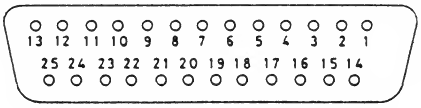

FIGURE 7-5. CN4 PIN LOCATIONS

TABLE 7-7. CN4 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	-	-	NC (unused)
2	$\overline{\text{TXD}}$	O	Transmitted Data
3	$\overline{\text{RXD}}$	I	Received Data
4	RTS	O	Received Data
5	CTS	I	Clear to Send
6	DTR	I	Data Set Ready
7	SG	-	Signal Ground
8	CD	I	Carrier Detect
9-19	-	-	NC (unused)
20	DTR	O	Data Terminal Ready
21	-	-	NC (unused)
22	RI	I	Ring Indicator
23-24	-	-	NC (unused)

NOTE: Signal direction is as viewed from the MCY board.

Connector CN5

Use : Monitor port
Type: HONDA, GMM-A9GDFDB

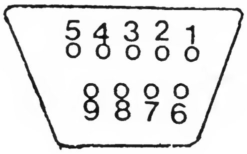

FIGURE 7-6. CN5 PIN LOCATIONS

TABLE 7-8. CN5 PIN ASSIGNMENT (Color Mode)

PIN No.	SIGNAL	DIRECTION	DESCRIPTION
1	GND	-	Ground
2	GND	-	Ground
3	R	O	Red
4	G	O	Green
5	B	O	Blue
6	I	O	Intensity
7	-	-	(Not used)
8	H	O	Horizontal Sync Drive
9	V	O	Vertical Sync Drive

TABLE 7-9. CN5 PIN ASSIGNMENT (Monochrome Mode)

PIN No.	SIGNAL	DIRECTION	DESCRIPTION
1	GND	-	Ground
2	GND	-	Ground
3	-	-	-
4	-	-	-
5	-	-	-
6	INT	O	Intensity
7	VIDEO	O	Video
8	H	O	Horizontal Sync Drive
9	V	O	Vertical Sync Drive

NOTE: Signal direction is as viewed from the MCY board.

Connector CN6

Use : Composit Video Interface
Type: HOSHIDENKI, JPJ-2545-01-510

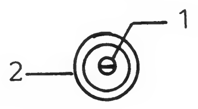

FIGURE 7-7. CN6 PIN LOCATIONS

TABLE 7-10. CN6 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	Video	O	Composit Video Signal
2	GND	-	Ground

Connector CN8

Use : Keyboard port
Type: HOSHIDENKI, TCS5040-18-1011

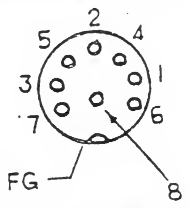

FIGURE 7-8. CN8 PIN LOCATIONS

TABLE 7-11. CN8 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	KBDCLK	I/O	Keyboard Clock
2	KBDDATA	I/O	Keyboard Data
3	KBDRST	O	Keyboard Reset
4	KBDGND	-	Ground
5	KBD+5	-	+5 V for Keyboard
6	KBDCNT	I/O	Data Keyboard Control
7	KBDSTP	I	Keyboard Stop
8	KBDTST	I/O	Keyboard Test

NOTE: Signal direction is as viewed from the MCY board.

Connector CN9,10

Use : FDD control port
Type: DDK, FRC5-C34S53T-OS (D20)

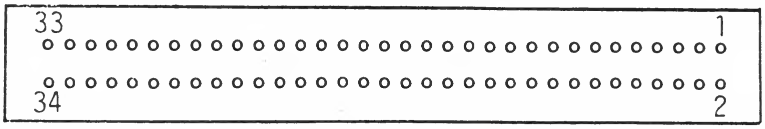

FIGURE 7-9. CN9 PIN LOCATIONS

TABLE 7-12. CN9,10 PIN ASSGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	MODE	O	Drive Speed Mode
4	DS CHNG	I	Disk Change
6	DRSEL 3	O	Drive Select 3
8	INDEX	I	Index Pulse
10	DRSEL 0	O	Drive Select 2
12	DRSEL 1	O	Drive Select 1
14	DRSEL 2	O	Drive Select 2
16	MT ON	O	Motor on
20	STEP	O	Step Pulse
22	WR DATA	O	Write Data
24	WR GATE	O	Write Gate
26	TRK 00	I	Track 00
28	WR PRT	I	Write Protect
30	RD DATA	I	Read Data
32	SD SEL	O	Side Select
34	NC	-	Ready
1-33	GND	-	Ground

NOTE: Signal direction is as viewed from the MCY board.

Connector CN11

Use : To power SW and LED
Type: ELCO, 00-8283-0512-00-000

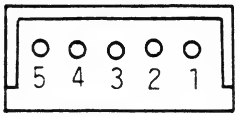

FIGURE 7-10. CN11 PIN LOCATIONS

TABLE 7-13. CN11 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	PNOFF	I	Power Off
2	PNON	I	Power On
3	GND	-	Ground
4	HSPD	O	Clock 7 MHz
5	LSPD	O	Clock 4 MHz

NOTE: Signal direction is as viewed from the MCY board.

Connector CN12

Use : To speaker
Type: ELCO, 00-8283-0212-00-000

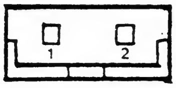

FIGURE 7-11. CN12 PIN LOCATIONS

TABLE 7-14. CN12 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	GND	-	Ground
2	SPD	O	Speaker Data

Connector CN13

Use : To battery
Type: JAE, IL-2P-S3FP2

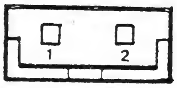

FIGURE 7-12. CN13 PIN LOCATIONS

TABLE 7-15. CN13 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	GND	-	Ground
2	+6 V	-	+6 V

NOTE: Signal direction is as viewed from the MCY board.

Connector CN14

Use : RAM card I/F board.
Type: HIROSE, PCN10-48S-2.54DSA

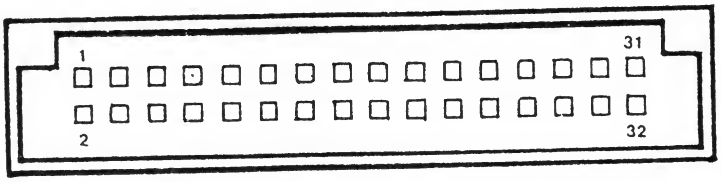

FIGURE 7-13. CN14 PIN LOCATIONS

TABLE 7-16. CN14 PIN ASSGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
A1	GND	-	Ground
A2	MDPL	O	Parity Low Bits
A3	AD13	I/O	Address & Data Bit 13
A4	AD10	I/O	Address & Data Bit 10
A5	AD7	I/O	Address & Data Bit 7
A6	AD4	I/O	Address & Data Bit 4
A7	AD1	I/O	Address & Data Bit 1
A8	+5 V	-	+5 V
A9	MA 8	O	Memory Address Bit 8
A10	MA 6	O	Memory Address Bit 6
A11	GND	-	Ground
A12	GND	-	Ground
A13	GND	-	Ground
A14	GND	-	Ground
A15	$\overline{\text{CAS}}$	O	Column Address Strobe
B1	MDPH	I/O	Parity High Bits
B2	AD15	I/O	Address & Data Bit 15
B3	AD12	I/O	Address & Data Bit 12
B4	AD9	I/O	Address & Data Bit 9
B5	AD6	I/O	Address & Data Bit 6
B6	AD3	I/O	Address & Data Bit 3
B7	AD0	I/O	Address & Data Bit 0
B8	+5 V	-	+5 V
B9	MA7	O	Memory Address Bit 7
B10	MA5	O	Memory Adderss Bit 5
B11	MA0	O	Memory Address Bit 0
B12	MA2	O	Memory Address Bit 2
B13	GND	-	

B14	$\overline{\text{RAS0}}$	O	Row Address Strobe 0
B15	$\overline{\text{RAS2}}$	O	Row Address Strobe 2
B16	$\overline{\text{WE}}$	O	Write Enable
C1	GND	-	
C2	AD14	I/O	Address & Data Bit 14
C3	AD11	I/O	Address & Data Bit 11
C4	AD8	I/O	Address & Data Bit 8
C5	AD5	I/O	Address & Data Bit 5
C6	AD2	I/O	Address & Data Bit 2
C7	+5 V	-	+5 V
C8	+5 V	-	+5 V
C9	+5 V	-	+5 V
C10	MA4	O	Memory Address Bit 4
C11	MA1	O	Memory Address Bit 1
C12	MA3	O	Memory Address Bit 3
C13	GND	-	Ground
C14	RAS1	O	Row Address Strobe 1
C15	RAS3	O	Row Address Strobe 3
C16	GND	-	Ground
A16	GND	-	Ground

NOTE: Signal direction is as viewed from the MCY board

Slot #1-#4

Use : Option card port #1-#4
Type: DDK, 226D-10031L2-2320

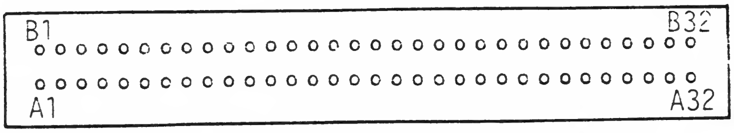

FIGURE 7-14. Slot #1-#4 PIN LOCATIONS

TABLE 7-17. SLOLT #1-#4 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
A1	$\overline{\text{IOCHCK}}$	I	I/O Channel Check
A2	D7	I/O	Data Bit 7
A3	D6	I/O	Data Bit 6
A4	D5	I/O	Data Bit 5
A5	D4	I/O	Data Bit 6
A6	D3	I/O	Data Bit 4
A7	D2	I/O	Data Bit 3
A8	D1	I/O	Data Bit 2
A9	D0	I/O	Data Bit 1
A10	IOCHRDY	I	Data Bit 0
A11	AEN	O	I/O Channel Ready
A12	A19	O	Address Latch Enable
A13	A18	O	Address Bit 19
A14	A17	O	Address Bit 18
A15	A16	O	Address Bit 17
A16	A15	O	Address Bit 16
A17	A14	O	Address Bit 15
A18	A13	O	Address Bit 14
A19	A12	O	Address Bit 13
A20	A11	O	Address Bit 12
A21	A10	O	Address Bit 11
A22	A9	O	Address Bit 10
A23	A8	O	Address Bit 9
A24	A7	O	Address Bit 8
A25	A6	O	Address Bit 7

A26	A5	O	Address Bit 6	
A27	A4	O	Address Bit 5	
A28	A3	O	Address Bit 4	
A29	A2	O	Address Bit 3	
A30	A1	O	Address Bit 1	
A31	A0	O	Address Bit 2	
B1	GND	-	Ground	
B2	RESETDRV	O	Reset Driver	
B3	+5 V	-	+5 V	
B4	IRQ2	I	Interrupt Request 2	
B5	-5VDC	-	-5 V	
B6	DRQ2	I	DMA Request 2	
B7	-12 V	-	-12 V	
B8	**WAKE UP**	-	**One of the Power ON Signal**	B
B9	+12 V	-	+12 V	
B10	GND	-	Ground	
B11	$\overline{\text{MEMW}}$	O	Memory Write Command	
B12	$\overline{\text{MEMR}}$	O	Memory Read Command	
B13	$\overline{\text{IOW}}$	O	I/O Write Command	
B14	$\overline{\text{IOR}}$	O	I/O Read Command	
B15	$\overline{\text{DACK3}}$	O	DMA Acknowledge 3	
B16	DRQ3	I	DMA Request 3	
B17	$\overline{\text{DACK1}}$	O	DMA Acknowledge 1	
B18	DRQ1	I	DMA Request 1	
B19	$\overline{\text{DACK0}}$	O	DMA Acknowledge 0	
B20	CLOCK	O	Clock (4.77 MHz duty 33%)	
B21	IRQ7	I	Interrupt Request 7	
B22	IRQ6	I	Interrupt Request 6	
B23	IRQ5	I	Interrupt Request 5	
B24	IRQ4	I	Interrupt Request 4	
B25	IRQ3	I	Interrupt Request 3	
B26	$\overline{\text{DACK2}}$	O	DMA acknowledge 2	
B27	T/C	O	Terminal Count	
B28	ALE	O	Address Latch Enable	
B29	+5 V	-	+5 V	
B30	OSC	O	Oscillator (14.31818 MHz)	
B31	GND	-	Ground	

Slot #5

Use : Option card port #5
Type: DDK, 226D-10031L2-2320

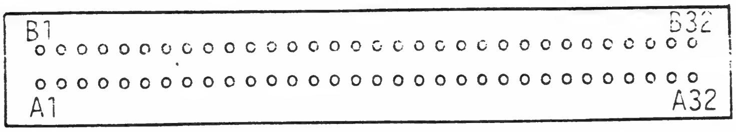

FIGURE 7-15. SLOT #5 PIN LOCATIONS

TABLE 7-18. SLOT #5 PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
B1	GND	-	Ground
B2	RESETDRV	O	Reset Driver
B3	+5 V	-	+5 V
B4	IRQ2	I	Interrupt Request 2
B5	-5VDC	-	-5 V
B6	DRQ2	I	DMA Request 2
B7	-12 V	-	-12 V
B8	WAKE UP	-	One of the Power ON Signal
B9	+12 V	-	+12 V
B10	GND	-	Ground
B11	$\overline{\text{MEMW}}$	O	Memory Write Command
B12	$\overline{\text{MEMR}}$	O	Memory Read Command
B13	$\overline{\text{IOW}}$	O	I/O Write Command
B14	$\overline{\text{IOR}}$	O	I/O Read Command
B15	$\overline{\text{DACK3}}$	O	DMA Acknowledge 3
B16	DRQ3	I	DMA Request 3
B17	$\overline{\text{DACK1}}$	O	DMA Acknowledge 1
B18	DRQ1	I	DMA Request 1
B19	$\overline{\text{DACK0}}$	O	DMA Acknowledge 0
B20	CLOCK	O	Clock (4.77 MHz duty 33%)
B21	IRQ7	I	Interrupt Request 7
B22	IRQ6	I	Interrupt Request 6
B23	IRQ5	I	Interrupt Request 5
B24	IRQ4	I	Interrupt Request 4
B25	IRQ3	I	Interrupt Request 3
B26	$\overline{\text{DACK2}}$	O	DMA acknowledge 2
B27	T/C	O	Terminal Count
B28	ALE	O	Address Latch Enable
B29	+5 V	-	+5 V
B30	OSC	O	Oscillator (14.31818 MHz)
B31	GND	-	Ground

NOTE: The pin definition of the side A is similar to the slot #1-#4.

7.4 I/O MAP

Table 7-18 shows the I/O port map. Each I/O port configuration is described following the table.

TABLE 7-18. I/O PORT MAP

FUNCTION	I/O ADDRESS	READ	WRITE
DMAC	000	Not Used	Not Used
	001	Not Used	Not Used
	002	Ch.1 Current Address	Ch.1 Base Address
	003	Ch.1 Word Count	Ch.1 Word Count
	004	Ch.2 Current Address	Ch.2 Base Address
	005	Ch.2 Word Count	Ch.2 Word Count
	006	Ch.3 Current Address	Ch.3 Base Address
	007	Ch.3 Word Count	Ch.3 Word Count
	008	Status Register	Command Register
	009	--------------------	Request Register
	00A	--------------------	Single Mask Register
	00B	--------------------	Mode Register
	00C	--------------------	Clear Byte Pointer
	00D	Temporary Register	Master Clear
	00E	--------------------	Clear Mask Register
	00F	--------------------	All Mask Register Set
INTERRUPT CONTROL	020	IRR, ISR (high priority)	OCW2, OCW3, ICW1
	021	INT, Mask Register (high priority)	INT, Mask Register ICW2, ICW4
TIMER COUNTER	040	Timer 0	Timer 0
	041	Timer 1	Timer 1
	042	Timer 2	Timer 2
	043	--------------------	Control Word Register
KB/ DIP SW	060	Key Input Register	-------------------
	061	Peripheral Control	Peripheral Control
	062	DIP SW, etc.	-------------------
DMA PAGE REGISTER	081	--------------------	DMA Ch.2 Page Register
	082	--------------------	DMA Ch.3 Page Register
	083	--------------------	DMA Ch.1 Page Register
NMI MASK	0A0	--------------------	NMI Enable Register
ASYNC COMMUNICA (second)	2F8	Receive Buffer Register	Transmit Buffer Register
	2F9	INTR, Enable Register	INTR. Enable Register
	2FA	INTR, ID Register	-------------------
	2FB	Line Control Register	Line Control Register
	2FC	MODEM Status Register	MODEM Control Register
	2FD	Line Status Register	Line Status Register
	2FE	MODEM Status Register	-------------------
B/O MONITOR	3B4	--------------------	CRTC Index Register
	3B5	CRTC Data Register	CRTC Data Register
	3B8	--------------------	CRT Control Port
	3BA	CRT Status Register	-------------------
	3BF	--------------------	Configuration SW
	378	Output Data Register	Output Date Register

PRINTER	379	Status Register	--------------------	
	37A	Command Register	Command Register	
	3BC	Output Data Register	Output Data Register	
PRINTER	3BD	Output Data Register	--------------------	
	3BE	Command Register	Command Register	
	(NOTE: Either one of printer ports 3BD and 3BE is selected by SW4; however, both are not used at the same time.)			
	3D4	--------------------	Index Register	
COLOR MONITOR	3D5	Data Register	Data Register	
	3D8	--------------------	Mode Control Register	
	3D9	--------------------	Color Select Register	
	3DA	Status Register	--------------------	
	3F2	--------------------	Digital Output Register	
	3F4	Main Status Register	--------------------	
	3F5	Data Register	Data Register	
	3F8	Register Buffer Register	Transmit Buffer Register	
	3F9	INTR. Enable Register	INTR.Enable Register	
ASYNC COMMUNICATION (primary)	3FA	INTR. ID Register	--------------------	
	3FB	Line Control Register	Line Control Register	
	3FC	MODEM Control Register	MODEM Control Register	
	3FD	Line Status Register	Line Status Register	
	3FE	MODEM Status Register	--------------------	
MONITOR	11B0	--------------------	Video Configuration Register	
MONITOR	11B1	Font Select Register	Frontselect & Color Phase	
RTC	11B4	--------------------	Timer Address Register	
RTC	11B5	RTC Registers	RTC Register	
DIP.SW	11B6	DIP Switches	--------------------	
CLOCK	11B7	--------------------	Clock & Wait Control	
POWER	11B8	Power Status Register	Power Control Register	
ASYNCsel	11B9	--------------------	Peripheral Select Register	B
FDD MODE	11BA	FD Mode Register	FD Mode Register	
INT	11BC	IRR, ISR	OCW2, OCW3	
INT	11BD	Interrrupt Make Register	Interrrupt Make Register	
CONTROL	11BE	Select Register	--------------------	

7.4.2 I/O Port Configuration

This section describes bit map of each I/O port in detail. I/O port configuration is as follows.

```
***********************************************
*                                             *
*    Device Name          :DMAC 8237A-5 (40)  *
*                          GAMYDM (4N)        *
*    Function             :DMA controller     *
*    I/O Address          :000 - 00FH         *
*                                             *
***********************************************
```

*** I/O address 002H (Read) Ch.1 current address ***********

DMAC

7	6	5	4	3	2	1	0
CAR17	CAR16	CAR15	CAR14	CAR13	CAR12	CAR11	CAR10

DMA Ch.1 Current Address (Low and High Byte)

NOTE: DMA from Option slot

*** I/O address 002H (Write) Ch.1 base address ************

DMAC

7	6	5	4	3	2	1	0
BAR17	BAR16	BAR15	BAR14	BAR13	BAR12	BAR11	BAR10

DMA Ch. Base Address (Low and High Byte)

NOTE: DMA from Option slot

*** I/O address 003H (Read)(Write) Ch.1 word count **********

DMAC

7	6	5	4	3	2	1	0
WCR17	WCR16	WCR15	WCR14	WCR13	WCR12	WCR11	WCR10

DMA Ch.1 Word Counter (Low and High Byte)

NOTE: DMA from Option slot

*** I/O address 004h (Read) Ch.2 current address **********

DMAC

7	6	5	4	3	2	1	0
CAR27	CAR26	CAR25	CAR24	CAR23	CAR22	CAR21	CAR20

DMA Ch.2 Current Address (Low and High Byte)

NOTE: DMA from FDC or Option slot

*** I/O address 004H (Write) Ch.2 base address ************

DMAC

7	6	5	4	3	2	1	0
BAR27	BAR26	BAR25	BAR24	BAR23	BAR22	BAR21	BAR20

DMA Ch.2 Base Address (Low from FDC or Option slot)

NOTE: DMA from FDC or Option slot

*** I/O address 005H (Read)(Write) Ch.2 word count **********

DMAC

7	6	5	4	3	2	1	1
WCR27	WCR26	WCR25	WCR24	WCR23	WCR22	WCR21	WCR20

DMA Ch.2 Word Counter (Low and High Byte)

NOTE: DMA from FDC or Option slot)

*** I/O address 006H (Read) Ch.3 current address ************

DMAC

7	6	5	4	3	2	1	0
CAR37	CAR36	CAR35	CAR34	CAR33	CAR32	CAR31	CAR30

DMA Ch.3 Current Address (Low and High Byte)

NOTE: DMA from HDC or Option slot

*** I/O address 006H (Write) Ch.3 base address ************

DMAC

7	6	5	4	3	2	1	0
BAR37	BAR36	BAR35	BAR34	BAR33	BAR32	BAR31	BAR30

DMA Ch.3 Base Address (Low and High Byte)

NOTE: DMA from HDC or Option slot

*** I/O address 007H (Read)(Write) Ch.3 word count ***********

DMAC

7	6	5	4	3	2	1	0
WCR37	WCR36	WCR35	WCR34	WCR33	WCR32	WCR31	WCR30

DMA Ch.3 Word Counter (Low and High Byte)

NOTE: DMA from HDC or Option slot

*** I/O address 008H (Read) Status Register ***************

DMAC

```
   7       6       5       4       3       2       1       0

 RQDMA3  RQDMA2  RQDMA1    -     DMATC3  DMATC2  DMATC1    -
   |       |       |               |       |       |
   |       |       |               |       |       |
   |       |       |               |       |     Ch.1 Reached TC
   |       |       |               |       +---  Ch.2 Reached TC (FDC)
   |       |       |               +-----------  Ch.3 Reached TC (HDC)
   |       |       +---------------------------  Ch.1 DMA request
   |       +-----------------------------------  Ch.2 DMA request (FDC)
   +-------------------------------------------  Ch.3 DMA request (HDC)
```

```
*** I/O address    008H (Write)    Command Register *************

DMAC
     7    6    5    4    3     2    1    0

   DACK DREQ EXTW PRIO TIMNG ENBL AHLD MTOM
     |    |    |    |    |     |    |    |
     |    |    |    |    |     |    |    |
     |    |    |    |    |     |    |  0: Memory to Memory Disable
     |    |    |    |    |     |    +- 0: Ch.0 address hold Disable
     |    |    |    |    |     +------ 0: Controller Enable
     |    |    |    |    +------------ 0: Normal timing
     |    |    |    +----------------- 0: Fixed priority
     |    |    +---------------------- 1: Extended write
     |    +--------------------------- 0: DREQ signal active HIGH
     +-------------------------------- 0: DACK signal active LOW
```

```
*** I/O address    009H (Write)    Request Register *************

DMAC
    7   6   5   4   3     2      1      0

    -   -   -   -   -   SETBIT CHSEL1 CHSEL0
    |   |   |   |   |     |      |      |
    +---+---+---+---+     |      |      |
                    |     |      |   1: Ch.1, 0: Ch.2, 1: Ch.3
                    |     |      +---0:       1:       1:
                    |     |
                    |     +---------- 0: Reset, 1: Set DMA Request
                    +---------------- Don't care
```

```
*** I/O address    00BH (Write)    Mode Register *************

DMAC
  7     6     5      4    3      2      1      0

MODE1 MODE0 INCDEC AUTO DIRCT1 DIRCT0 CHSEL1 CHSEL0
  |     |     |     |     |      |      |      |
  |     |     |     |     |      |      |      |
  |     |     |     |     |      |      |  1:Ch.1, 0:Ch.2, 1:Ch.3
  |     |     |     |     |      |      +- 0:     1:      1:
  |     |     |     |     |      +- 0: Verify, 1: Write, 0: Read,
  |     |     |     |     +-------- 0:        0:   Mem  1:   Mem
  |     |     |     +-------------- Auto init. 0:Disable, 1:Enable
  |     |     +-------------------- Address 0: Inc., 1: Dec.
  |     +-------------------------- 0:Demand, 1:Single, 0:Block
  +-------------------------------- 0:        0:        1:
```

*** I/O address 00CH (Write) Clear Byte Pointer F.F. *********

DMAC

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Note: What ever you write into this port, DMA controller will clear the byte pointer F.F. Whitch is using for read/write operation of address register or word counter.

*** I/O address 00DH (Write) Temporary Register *************

DMAC

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Note: Temporary register is used for holding data while the DMAC is transfering a data from memory to memory. You will not be able to access this register.

*** I/O address 00DH (Write) Master Clear **************

DMAC

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Note: This port does not have the same effect as the hardware reset. The Command, Status, Request, Temporary and Internal First/Last F.F. reg. will be cleared and Mask register will be set.

*** I/O address 00EH (Write) Clear Mask Register ***********

DMAC

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Note: This Command clears the mask bit of all four channels, enabling them to accept DMA request.

```
*** I/O address   00FH (Write)  All Mask Register Set **********

DMAC
 7   6   5   4   3      2      1      0

 -   -   -   -  MASK3  MASK2  MASK1   -
 |   |   |   |   |      |      |      |
 +---+---+---+   |      |      |      |
         |       |      |      |   Don't care
         |       |      |      +-- Ch.1 Mask bit 0: Clear, 1: Set
         |       |      +--------- Ch.2 Mask bit 0: Clear, 1: Set
         |       +---------------- Ch.3 Mask bit 0: Clear, 1: Set
         +------------------------ Don't care
```

```
*********************************************
*                                           *
*     Device Name : GAMYIO (4K)             *
*     Function    : Interrupt controller    *
*     I/O Address : 020-021H                *
*                                           *
*********************************************
```

```
*** I/O address   020H (Read)  Interrupt Reqest Register ********

INTERRUPT #1
   7    6    5    4    3    2    1    0

  IRR7 IRR6 IRR5 IRR4 IRR3 IRR2 IRR1 IRR0
   |    |    |    |    |    |    |    |
   |    |    |    |    |    |    |    |
   |    |    |    |    |    |    |  Intr. Req. bit of Timer
   |    |    |    |    |    |    +- Intr. Req. bit of Keyboard RXD
   |    |    |    |    |    +------ Intr. Req. bit of Reserved
   |    |    |    |    +----------- Intr. Req. bit of Async (second)
   |    |    |    +---------------- Intr. Req. bit of Async (primary)
   |    |    +--------------------- Intr. Req. bit of HDC
   |    +-------------------------- Intr. Req. bit of FDC
   +------------------------------- Intr. Req. bit of Printer
```

Note: Before this register to be accessed, you should write OCW3 command onto 020H.

```
*** I/O address   020H (Read)   In Service Register ***********

INTRRUPT #1
  7    6    5    4    3    2    1    0

 ISR7 ISR6 ISR5 ISR4 ISR3 ISR2 ISR1 IRS0
  |    |    |    |    |    |    |    |
  |    |    |    |    |    |    |    |
  |    |    |    |    |    |    |    |
  |    |    |    |    |    |    |  In Service bit of Timer
  |    |    |    |    |    |    +- In Service bit of Keyboard RXD
  |    |    |    |    |    +------ In Service bit of Reserved
  |    |    |    |    +----------- In Service bit of Async (second)
  |    |    |    +---------------- In Service bit of Async (primary)
  |    |    +--------------------- In Service bit of HDC
  |    +-------------------------- In Service bit of FDC
  +------------------------------- In Service bit of Printer
```

Note: Before accessing this register , you should write OCW3 command onto 020H.

```
*** I/O address     020H (Write)    ICW1 ***********************

INTERRUPT #1,#2
    7    6    5    4    3    2    1    0

    -    -    -    1    -    -    -    -
```

Note: ICW1 resets interrupt controller. Two byte data following this command (ICW2,ICW3,ICW4) are ignored.

```
*** I/O address      020H (Write)    OCW2 ***********************

INTERRUPT #1
    7    6    5   4    3     2       1       0

    -   SEOI NEOI  0    0   INTLV2  INTLV1  INTLV0
    |    |    |              |       |       |
    |    |    |              |       |       |
    |    |    |              +-------+-------+
    |    |    |                      |
    |    |    |                      +----- Intr. level
    |    |    +---------------------------- Normal EOI Mode
    |    +--------------------------------- Special EOI Mode
    +-------------------------------------- Don't care
```

```
*** I/O address     020H (Write)   OCW3 ***********************

INTERRUPT #1
    7   6    5   4  3  2    1    0

    -  ESMM SMM  0  1  -   RRB  ISIR
    |   |    |              |    |
    |   |    |              |    |
    |   |    |              |  0: IRR, 1: ISR, X: if bit1=0
    |   |    |              +- Read register 0: Disable, 1:Enable
    |   |    +---------------- Special Mask 0: Rest, 1: Set
    |   +--------------------- Special Mask Mode 1: Enable
    |                                            0: Disable
    +------------------------- Don't care
```

```
*** I/O address  021H (Read)(Write) Interrupt Mask Register *****

INTERRUPT #1
    7     6     5     4     3     2     1     0

  IMB7  IMB6  IMB5  IMB4  IMB3  IMB2  IMB1  IMB0


         Interrupt Mask Bit
           0: Clear mask
           1: Set mask
```

```
*********************************************
*                                           *
*    Device Name : Timer/Counter 8253 (2T)  *
*    Function    : Keyboard, Peripheral control *
*    I/O Address : 060-062H                 *
*                                           *
*********************************************
```

```
*** I/O address   040H (Read)(Write)  Timer Counter 0 ***********

TIMER
    7   6   5   4   3   2   1   0

    -   -   -   -   -   -   -   -
    |   |   |   |   |   |   |   |
    +---+---+---+---+---+---+---+------- TIMER0
```

Note: This is a count or a Value for Timer 0 the general purpose clock. (EQUITY II default : 0)

```
*** I/O address  041H  (Read)(Write) Timer Counter 1 ***********

TIMER
    7   6   5   4   3   2   1   0

    -   -   -   -   -   -   -   -
    |   |   |   |   |   |   |   |
    +---+---+---+---+---+---+---+------- TIMER1
```

Note: You can set the interval timer whitch refreshes the RAM of the extended slot by this timer counter 1.
You have to set 12H.

```
*** I/O address  042H (Read)(Write) Timer 2 Count Value ********

TIMER
    7   6   5   4   3   2   1   0

    -   -   -   -   -   -   -   -
    |   |   |   |   |   |   |   |
    +---+---+---+---+---+---+---+------- TIMER2
```

Note: This is a count or a Varue for Timer 2 the sound Generation timer

```
*** I/O address   043H (Write) Control Word register ************

TIMER
   7      6     5    4     3      2      1      0

 TMSEL1 TMSEL0 RLB1 RLB0 MDSEL2 MDSEL1 MDSEL0   0
   |      |     |    |     |       |     |      |
   |      |     |    |     |       |     |      |
   |      |     |    |     |       |     |      |
   |      |     |    |     |       |     |      +- Binaly only
   |      |     |    |     |       |     +- 0:Mode,  1:Mode, 0:Mode
   |      |     |    |     |       +------- 0: 0    0: 1    1: 2
   |      |     |    |     +--------------- 0:      0:      X:
   |      |     |    |
   |      |     |    |                      1:Mode, 0:Mode, 1:Mode,
   |      |     |    |                      1: 3    0: 4    0: 5
   |      |     |    |                      X:      1:      1:
   |      |     |    +------ 0:Counter, 1:LSB   0:MSB   1:LSB and
   |      |     +----------- 0:Latch    0:only, 1:only, 1:MSB
   |      +----------------- 0:Timer0, 1:Timer2, 0:Timer1, 1:illegal
   +------------------------ 0:        0:        1:        1:
```

```
*************************************************
*                                               *
*    Device Name : GAMYOS (3N)                  *
*    Function    : Keyboard, Peripheral control *
*    I/O Address : 060-062H                     *
*                                               *
*************************************************

*** I/O address   060H (Read)   Key Input Register ************

KB/DIP
    7   6   5   4   3   2   1   0

                KEYIN

 Note: Keyboard scan code data


*** I/O address  061H (Read)(Write)  Peripheral Control ********

KB/DIP
  7     6      5      4     3     2    1     0

KBENB KBCLK IOCHKEN PRTYEN SWSEL  -  SPDAT TIMGT
  |     |      |      |     |          |     |
  |     |      |      |     |          |     |
  |     |      |      |     |          |     |
  |     |      |      |     |          |  Enable Timer 2 Gate
  |     |      |      |     |          +- Speaker Data
  |     |      |      |     +-- DIP SW. 0:Low nibble, 1:High nibble
  |     |      |      +-------- RAM Parity 0:Enable 1:Disable
  |     |      +--------------- I/O check 0:Enable 1:Disable
  |     +---------------------- KB clock 0:Low, 1:Active
  +---------------------------- KB buffer 0:Enable, 1:Clear


 I/O address     062H (Read)          DIP SW. and etc

KB/DIP
  7       6       5      4     3     2     1     0

PRTYER IOCHKER TIM2IN SPKIN SW4/8 SW3/7 SW2/6 SW1/5
  |       |       |      |     |     |     |     |
  |       |       |      |     |     |     |     |
  |       |       |      |     |     |     | SW1.. Drive type,
  |       |       |      |     |     |     |       /SW5.. Display
  |       |       |      |     |     |    SW2.. - ,/SW6..   Select
  |       |       |      |     |     |
  |       |       |      |     |    SW3.. RAM size,/SW7.. FDD
  |       |       |      |     +-- SW4.. "1",      /SW8..   Select
  |       |       |      |
  |       |       |      +-------- Speaker output
  |       |       +--------------- Timer 2 output data
  |       +----------------------- I/O check error bit
  +------------------------------- RAM Parity error bit
```

```
*************************************************
*                                               *
*    Device Name : DMAC 8237-5 (40)             *
*                  GAMYDM (4N)                  *
*    Function    : Setting the DMA page register*
*    I/O Address : 081-083H                     *
*                                               *
*************************************************

*** I/O address    081H (Write)  DMA Ch.2 PAGE Register *********

PAGE REG
    7   6   5   4    3      2      1      0

    -   -   -   - DMAC29 DMAC28 DMAC27 DMAC26
    |   |   |   |    |      |      |      |
    +---+---+---+    |      |      |      |
                |    |      |      |      |
                |    |      |      |    DMA CH.2 Address bit A16
                |    |      |      +--- DMA CH.2 Address bit A17
                |    |      +---------- DMA CH.2 Address bit A18
                |    +----------------- DMA CH.2 Address bit A19
                +---------------------- Don't care

*** I/O address   082H (Write)   DMA Ch.3 PAGE Register ************

PAGE REG
    7   6   5   4    3      2      1      0

    -   -   -   - DMAC39 DMAC38 DMAC37 DMAC36
    |   |   |   |    |      |      |      |
    +---+---+---+    |      |      |      |
                |    |      |      |      |
                |    |      |      |    DMA CH.3 Address bit A16
                |    |      |      +--- DMA CH.3 Address bit A17
                |    |      +---------- DMA CH.3 Address bit A18
                |    +----------------- DMA CH.3 Address bit A19
                +---------------------- Don't care

*** I/O address   083H (Write)   DMA Ch.1 PAGE Register ***********

PAGE REG
    7   6   5   4    3      2      1      0

    -   -   -   - DMAC19 DMAC18 DMAC17 DMAC16
    |   |   |   |    |      |      |      |
    +---+---+---+    |      |      |      |
                |    |      |      |      |
                |    |      |      |      +- DMA CH.1 Address bit A16
                |    |      |      +-------- DMA CH.1 Address bit A17
                |    |      +--------------- DMA CH.1 Address bit A18
                |    +---------------------- DMA CH.1 Address bit A19
                +--------------------------- Don'T care
```

```
***************************************************
*                                                 *
*     Device Name : GAMYMC (7L)                   *
*     Function    : Setting the DMA page register *
*     I/O Address : 0A0H                          *
*                                                 *
***************************************************

*** I/O address   0A0H (Write)   NMI Enable register ***********

NMI
   7      6    5    4    3    2    1    0

  NMIEN   -    -    -    -    -    -    -
   |      |    |    |    |    |    |    |
   |      +----+----+----+----+----+----+-- Don't care
   |
   +--------------------------------------- NMI 0: Disable, 1: Enable

Note : 2F8h --- 2FEh ==> Same as 3F8h --- 3FEh
```

```
*************************************************
*                                               *
*    Device Name : CRTC MB89322 (2H)            *
*                  GAMYUA (1L)                  *
*                  GAMYUD (2D)                  *
*    Function    : B/W Monitor                  *
*    I/O Address : 3B4-3BFH                     *
*                                               *
*************************************************

*** I/O address  3B4H (Write)  CRTC INDEX Register *************

CRTC (monochrome)
    7   6   5    4      3      2      1      0

               REGAD4 REGAD3 REGAD2 REGAD1 REGAD0
    ¦   ¦   ¦    ¦      ¦      ¦      ¦      ¦
    +---+---+    +------+------+------+------+
            ¦                         ¦
            ¦                       CRTC R0-R17  Register Number
            ¦
            +---------------------- Don't care


*** I/O address  3B5H (Read)(Write)  CRTC Data Register ********

CRTC (monochrome)
    7       6      5     4      3      2      1     0

  CMNDR7 CMNDR6 CMNDR5 CMNDR4 CMNDR3 CMNDR2 CMND1 CMNDR0


  Note : CRTC Command, Parameter (see CRTC manual)


*** I/O address   3B8H (Write)   CRTC control port ***********

CRTC (monochrome)
    7    6   5    4   3   2    1    0

  P1/P0  -  BLEN  -  VEN  -  TX/GR  -
    ¦        ¦        ¦        ¦
    ¦        ¦        ¦        ¦
    ¦        ¦        ¦        ¦
    ¦        ¦        ¦        0: Text mode, 1: Graphic mode
    ¦        ¦        +------- 0: Blink the screen, 1: activates
    ¦        +---------------- 0: Blink off, 1: Blink on
    +------------------------- 0: Page 0, 1: Page 1
```

```
*** I/O address    3BAH (Read)   CRT status port **************

CRTC (monochrome)
    7    6   5   4    3    2   1   0

  VSYNC  -   -   -  VIDEO  -   -  HSYNC
    |    |   |   |    |    |   |   |
    |    +---+---+    |    +---|   |
    |        |        |        |   |
    |        |        |        |  0: Normal Chr., 1: Sync area
    |        |        |       Don't care
    |        |        +------ 0: Dots off, 1: Dots on
    |        +--------------- Don't care
    +------------------------ 0: Vertical retrace, 1: active disp
```

```
*************************************************
*                                               *
*    Device Name : GAMYIO (4K)                  *
*    Function    : Printer controller           *
*    I/O Address : 378-37AH                     *
*                  3BC-3BEH                     *
*                                               *
*************************************************
```

```
*** I/O address   3BCH (Read)(Write)   Output Data Register ******

PRINTER
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    |    |    |    |    |    |    |    |
    +----+----+----+----+----+----+----+-----  PRNDT
```

Note : Out put data to a printer.

```
*** I/O address   3BDH (Read)    Printer Status Register *********

PRINTER
    7    6    5    4     3     2    1    0

  BUSY  ACK PERR SELIN EROR    -    -    -
    |    |    |    |     |     |    |    |
    |    |    |    |     |     +----+----+----- Don't care
    |    |    |    |     +------- 0:Error        1:not Error
    |    |    |    +------------- 0:not select   1:Selected
    |    |    +------------------ 0:Normal       1:Out of paper
    |    +----------------------- 0:Acknowledge 1:no response
    +---------------------------- 0:Busy         1:Ready
```

```
*** I/O address   3BEH (read)(write)   Command register ***********

PRINTER
    7    6    5    4     3     2    1    0

    -    -    - IRQEN SELOT INIT AUTO STRB
    |    |    |    |     |     |    |    |
    +----+----+    |     |     |    |    |
              |    |     |     |    |    |
              |    |     |     |    |    |
              |    |     |     |    |    0: No operation 1: Strobe
              |    |     |     |   0: Not autofeed,1: Autofeed
              |    |     |     +-- 0: Initialize,   1: No operation
              |    |     +-------- 0: Not select    1: Select
              |    +-------------- 1: Enable INTR, 0: Disable INTR
              +------------------- Don't care
```

```
*************************************************
*                                               *
*    Device Name : CRTC MB89322 (2H)            *
*                  GAMYVA (1L)                  *
*                  GAMYVD (2D)                  *
*    Function    : Color Monitor                *
*    I/O Address : 3D4-3DAH                     *
*                                               *
*************************************************
```

```
*** I/O address   3BFH (Write)   Hercules Configuration SW. *****

CRTC (monochrome)
     7     6    5    4    3    2     1        0

     -     -    -    -    -    -   MASKP1  PREV.GR
     |     |    |    |    |    |     |        |
     +-----+----+----+----+----+     |        |
                               |     |     0: Character mode only,
                               |     |     1: can set Graphic mode
                               |   0: Mask page 1,
                               |   1: Page 1 into Memory
                               +-- Don't care
```

```
*** I/O address    3D4H (Write)      INDEX Register ************

CRTC (color)
    7    6    5     4       3      2      1      0

    -    -    -   REGAD4  REGAD3 REGAD2 REGAD1 REGAD0
    |    |    |     |       |      |      |      |
    +----+----+     +-------+------+------+------+
              |                    |
              |            CRTC R0-R17 Register Number
              +----------- Don't care
```

```
*** I/O address   3D4H (Write)     INDEX Register *************

CRTC (color)
    7      6      5      4      3      2      1     0

 CMNDR7 CMNDR6 CMNDR5 CMNDR4 CMNDR3 CMNDR2 CMND1 CMNDR0


      Note : CRTC Command Parameter (see CRTC manual)
```

```
*** I/O address   3D8H (Write)   Mode Control Register *********

CRTC (color)
  7   6    5   4   3   2  1   0

  -   -  BLEN HGR VEN B/W GR HCH
  |   |    |   |   |   |   |  |
  +---+    |   |   |   |   |  |
      |    |   |   |   |   | 0: 40X25, 1: 80X25 alpha-numeric
      |    |   |   |   |  0: Alpha-numeric, 1: Graphic (320 dots)
      |    |   |   |   +- 0: Color mode, 1: Black and White
      |    |   |   +----- 0: Video disable, 1: Video enable
      |    |   +--------- 1: High resorution B/W mode
      |    +------------- 1: Blink, 0: Background intensity
      |              (Change the bit 7th mean of attribute byte)
      |
      +------------------ Don't care
```

```
*** I/O address   3D9H (Write)   Color Select Register *********

CRTC (color)
  7    6    5    4     3      2     1     0

  -    -    -    -   INTSFY  RED  GREEN  BLUE
                       |      |     |     |
                       |      |     |     |
                       |      |     |     +---- 1: Blue
                       |      |     +---------- 1: Green
                       |      +---------------- 1: Red
                       +----------------------- 1: High Intensity
                                                0: Low indensity

Note : Alpha-numeric mode Border Color Select
```

```
*** I/O address   3D9H (Write)    Color Select Register *********

CRTC (color)
  7   6   5     4     3     2    1    0

  -   -  CSEL BACKI INTSFY RED GREEN BLUE
          |           |     |    |    |
          |           |     |    |    |
          |           |     |    |   1: Blue
          |           |     |    +-- 1: Green      Back-ground
          |           |     +------- 1: Red         color select
          |           +------------- 1: High Intensity
          |                          0: Low Intensity
          +------------------------- Active set of color select

Note : Low resorution mode (320 X 200).
```

```
*** I/O address    3D9H (Write)    Color Select Register ********

CRTC (color)
   7   6   5   4    3      2     1     0

   -   -   -   -  INTSFY  RED  GREEN  BLUE
                    |      |     |     |
                    |      |     |     |
                    |      |     |   1: Blue
                    |      |     +-- 1: Green     Fore-ground
                    |      +-------- 1: Red         color select
                    +--------------- 1: High Intensify
                                     0: Low Intensify

Note : High resolution mode (640 X 200)
```

```
*** I/O address    3DAH (Read)    Status Register *************

CRTC (color)
   7   6   5   4    3     2     1     0

   -   -   -   -  VSYNC  LPSW  LPEN  DISP
                    |    |      |     |
                    |    |      |     |
                    |    |      |   0: In display area,
                    |    |      |   1: Not in display
                    |    |      |
                    |    |    always 0= L-pen trigger not occured
                    |    +--- always 1= light pen switch off
                    +-------- 1: Vertival retrace mode
```

```
*************************************************
*                                               *
*    Device Name : FDC 765AC (5H)               *
*    Function    : Floppy disk controller       *
*    I/O Address : 3F2-3F5H                     *
*                                               *
*************************************************
```

```
*** I/O address   3F2H (Write)   Digital output register ********

FDC
  7     6     5    4     3      2    1   0

MTEN4 MTEN3 MTEN2 MTEN1 ENDRQ RESET US1 US0
  |     |     |    |     |      |    |   |
  |     |     |    |     |      |    |   |
  |     |     |    |     |      |    |  0:Select     1:Select
  |     |     |    |     |      |    +- 0:  Drive A  0:  Drive B
  |     |     |    |     |      +-- 0: FDC reset, 1: FDC active
  |     |     |    |     +--------- DREQ,INTR 0:Disable, 1:Enable
  |     |     |    +--------------- Drive A motor enable
  |     |     +-------------------- Drive B motor enable
  |     +-------------------------- Drive C motor enable
  +-------------------------------- Drive D motor enable
```

```
*** I/O address   3F4H (Read)   Main Status Register ************

FDC
  7    6    5   4    3    2    1    0

 RQM  DIO  NDM  CB  DDB  DCB  DBB  DAB
  |    |    |   |    |    |    |    |
  |    |    |   |    |    |    |    |
  |    |    |   |    |    |    |  Drive A is in seek mode
  |    |    |   |    |    |    +- Drive B is in seek mode
  |    |    |   |    |    +------ Drive C is in seek mode
  |    |    |   |    +----------- Drive D is in seek mode
  |    |    |   +---------------- Command is in process
  |    |    +-------------------- Non-DMA mode
  |    +------------------------- Data transfer 0: to 1: from FDC
  +------------------------------ Request for Master
```

```
  I/O address     3F5H (Read)(Write)       Data Register

 FDC
      7    6    5    4    3    2    1    0

      -    -    -    -    -    -    -    -
      |    |    |    |    |    |    |    |
      +----+----+----+----+----+----+----+----- FDCDT
```

Note: Command or Parameter to FDC, Data or Parameter from FDC see FDC (UPD765) manual.

```
**************************************************
*                                                *
*    Device Name : GAMYIO (4K)                   *
*    Function    : Asychronous communication     *
*                  controller (primary)          *
*    I/O Address : 3F8-3FEH                      *
*                                                *
**************************************************
```

```
*** I/O addres   3F8H (Read)   Receive buffer register **********
                (2F8H)

ASYNC
     7    6    5    4    3    2    1    0

     -    -    -    -    -    -    -    -
     |    |    |    |    |    |    |    |
     +----+----+----+----+----+----+----+-------- RXDBF
```

Note : Received data buffer
You can read data from this register when the Divisor Latch access bit = 0: and the Line control register (3FBH) bit 7=0.

```
*** I/O addres   3F8H (Write)   Transmit buffer register ********
                (2F8H)

ASYNC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    |    |    |    |    |    |    |    |
    +----+----+----+----+----+----+----+--------  TXDBF
```

Note : Transmit data buffer
You can write data into this register when the Divisor Latch access bit = 0: and the Line control register (3FBH) bit 7=0.

```
*** I/O address  3F8H (Read)(Write)   Divisor Latch Reg.LSB *****
                 (2F8H)

ASYNC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    |    |    |    |    |    |    |    |
    +----+----+----+----+----+----+----+------- DVLBL
```

Note : Divisor Latch data (low byte)
You can read/write data from/into this register when the Divisor Latch access bit = 1: and the Line control register (3FBH) bit 7 = 1.

```
*** I/O address 3F9H (Read)(Write)   Divisor Latch reg. MSB *****
                (2F9H)

ASYNC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    |    |    |    |    |    |    |    |
    +----+----+----+----+----+----+----+------- DVLBH
```

Note : Divisor Latch data (High byte)
You can read/write data from/into this register when the Divisor Latch access bit = 1: and the Line control register (3FBH) bit 7 = 1.

```
*** I/O address  3F9H (Read)(Write) Interrupt enable register ***
                 (2F9H)

ASYNC
  7   6   5   4    3      2      1      0

  -   -   -   -  ENMDMI ENLINI ENTXDI ENRXDI
  |   |   |   |    |      |      |      |
  +---+---+---+    |      |      |      |
              |    |      |      |   Enable receive
              |    |      |      |       available interrupt
              |    |      |     Enable transmit empty interrupt
              |    |      +---- Enable receive Line status INTR
              |    +----------- Enable MODEM status interrupt
              +---------------- Don't care
```

Note: You can read/write data from/into this register when the Divisor Latch access bit = 0: and the Line control register (3FBH) bit 7 = 0.

```
*** I/O address  3FAH (Read)  Interrupt Identify register ********
                (2FAH)

ASYNC
 7  6  5  4    3    2    1    0

 -  -  -  -    -   IID1 IID0 PEND
 |  |  |  |    |    |    |    |
 +--+--+--+----+    |    |    |
               |    |    |    +- 0: INTR. pending, 1: none
               |    |    |
               |    |   0: MODEM   1: TXD    0: RXD    1: Recv
               |    +-- 0:   Stat  0:  Empt  1:  Avle  1:   Line
               |
               +------------ Don't care
```

```
*** I/O address  3FBH (Read)(Write)  Line control register *******
                (2FBH)

ASYNC
 7   6    5    4   3   2   1    0

DLAB BRKE STKP EPS PEN STB WLS1 WLS0
 |    |    |   |   |   |   |    |
 |    |    |   |   |   |   |    |
 |    |    |   |   |   |   |  0:5bit, 1:6bit, 0:7bit, 1:8bit
 |    |    |   |   |   |   +- 0:      0:      1:      1:
 |    |    |   |   |   +-- 0:1 Stop bit, 1:2 Stop bit
 |    |    |   |   +------ 0:Disable, 1: Enable Parity select
 |    |    |   +---------- 0:Odd, 1: Even parity check
 |    |    +-------------- Stick parity bit
 |    +------------------- 1:Set, 0: Reset Break
 +------------------------ Divisor latch access bit
                             1:3F8H,3F9H Divisor Latch reg .
                             0:3F8H,3F9H not Divisor Latch reg.
```

```
*** I/O address  3FCH (Read)(Write)  MODEM control register ******
                (2FCH)

ASYNC
  7   6   5   4     3    2     1    0

  -   -   - LOOP  OUT2   -   RTS  DTR
  |   |   |   |     |    |     |    |
  +---+---+   |     |    |     |   0:Non-active,
          |   |     |    |     |   1:Active DTR signal
          |   |     |    |    0:Non-active,
          |   |     |    |    1:Active request to send
          |   |     |    +--- Don't care
          |   |     +-------- 0:Interrupt disable, 1:Enable
          |   +-------------- 0:Noramal mode, 1:Loop-back test
          +------------------ Don't care
```

```
*** I/O address  3FDH (Read)(Write)  Line status register
                (2FDH)
ASYNC
  7    6     5     4    3   2   1   0

  -  TEMT  THRE  BINT  FE  PE  OE  DR
       |     |     |    |   |   |   |
       |     |     |    |   |   |   |
       |     |     |    |   |   |  Data ready
       |     |     |    |   |   +- Over run error
       |     |     |    |   +----- Parity error
       |     |     |    +--------- Framing error
       |     |     +-------------- Break interruput
       |     +-------------------- Transmit holding reg. empty
       +-------------------------- Transmitter empty
```

```
*** I/O address  3FEH (Read)(Write)  MODEM Status register *******
                (2FEH)
ASYNC
  7   6    5    4    3     2     1     0

DCD  RI  DSR  CTS  DDCD  TERI  DDSR  DCTS
  |   |    |    |    |     |     |     |
  |   |    |    |    |     |     |     |
  |   |    |    |    |     |     |   Delta clear to send
  |   |    |    |    |     |     +-- Delta data set ready
  |   |    |    |    |     +-------- Trailing edge ring indicator
  |   |    |    |    +-------------- Delta data carrier detect
  |   |    |    +------------------- Clear to send
  |   |    +------------------------ Data set ready
  |   +----------------------------- Ring indicator
  +--------------------------------- Data carrier detect
```

```
*** I/O address  11B0H (Write)  Video Configuration Register ****

MONITOR
     7         6     5    4  3  2    1     0
COLOR/MONO EXT/CMP MONO RVS VB VA 64/32 INH
     |         |     |    |  |  |    |     |
     |         |     |    |  |  |    |     |
     |         |     |    |  |  |    |    0:Normal display,
     |         |     |    |  |  |    |    1:Inhibit display
     |         |     |    |  |  |    +-- 0:VRAM 64K mode,
     |         |     |    |  |  |        1:VRAM 32K mode
     |         |     |    |  |  +-- VRAM address A13
     |         |     |    |  +----- VRAM address A14
     |         |     |    +-------- 0:Reverse OFF,
     |         |     |              1:Reserse ON
     |         |     +-- 1:Enable monochrome display mode
     |         +-------- 0:IBM compatible, 1:Extended mode
     +------------------ 0:Monochro enble, 1:Color enable
```

```
*** I/O address  11B1H (Read)  Font select register (not used) **

  7    6    5    4    3    2    1    0

  -    -    -    -    -    -    -  FONTJUMP
                                     |
                                     |
                                     +-- 0:7*7 1:5*7
```

```
*** I/O address 11B1H (Write)  FONT & COLOR PHASE SELECT ********

 7   6   5   4   3   2        1        0

 -   -   -   -   -   -   COLORPHASE FONTSEL
                              |        |
                              |        |
                              |        +--- 0 is set after reset
                              +------------ 0:7*7 1:5*7
```

```
*** I/O address  11B4H (Write)  Timer Address Register **********

   7    6     5      4      3      2      1      0

   -    -  RAMAD5 RAMAD4 RAMAD3 RAMAD2 RAMAD1 RAMAD0
```

Note : Internal RAM address RTC
   00H-0DH : Clock register
   0EH-3FH : Userd area

You must select the address to be accessed with out put the rerated data into 11B4H befor access 11B5H.

```
*** I/O address  11B5H (Read)(Write)   User RAM ****************

RTC
    7    6    5    4    3    2     1    0

    _    _    _    _    _    _     _    _
    ¦    ¦    ¦    ¦    ¦    ¦     ¦    ¦
    +----+----+----+----+----+-----+----+--- USRAM
```

Note : User RAM area on RTC
Write data 0EH - 3FH into 11B4H. befor accessing this area.

*** I/O address 11B5H (Read)(Write) Second Data ***********

```
RTC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
    +----+----+----+----+----+----+----+------ SECDT
```

Note : Second data to the calender clock
Write 00H into 11B4H befor access Second data to the calender clock.

*** I/O address 11B5H (Read)(Write) Second Alarm ***********

```
RTC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
    +----+----+----+----+----+----+----+------ ARSEC
```

Note : Second data to the alarm
Write 01H into 11B4H befor access Second data to the alarm.

*** I/O address 11B5H (Read)(Write) Minutes Data *************

```
RTC
    7    6    5    4    3    2    1    0

    -    -    -    -    -    -    -    -
    ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
    +----+----+----+----+----+----+----+------ MINDT
```

Note : Minutes data to the calendar clock
Write 02H into 11B4H befor access Minutes data to the calender clock.

```
*** I/O address   11B5H (Read)(Write)    Minutes Alarm *********

RTC
      7    6    5    4    3    2    1    0

      _    _    _    _    _    _    _    _
      ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
      +----+----+----+----+----+----+----+------- ARMIN
```

Note : Minutes data to the alarm
Write 03H into 11B4H befor access Minutes data to the alarm.

```
*** I/O address   11B5H (Read)(Write)   Hours Data ************

RTC
      7    6    5    4    3    2    1    0

      _    _    _    _    _    _    _    _
      ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
      +----+----+----+----+----+----+----+------- HORDT
```

Note : Hours data to the calendar clock
Write 04H into 11B4H befor access Houres data to the calender clock.

```
*** I/O address   11B5H (Read)(Write)   Hours Alarm ***************

RTC
      7    6    5    4    3    2    1    0

      _    _    _    _    _    _    _    _
      ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
      +----+----+----+----+----+----+----+------  ARHOR
```

Note : Hours data to the alarm
Write 05H into 11B4H befor access Hours data to the alarm.

*** I/O address 11B5H (Read)(Write) Week Data ****************

```
RTC
     7    6    5    4    3    2    1    0

     -    -    -    -    -    -    -    -
     ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
     +----+----+----+----+----+----+----+--------- WEKDT
```

Note : Week data to the calendar clock
Write 06H into 11B4H befor access Week data to the calender clock.

*** I/O address 11B5H (Read)(Write) Date Data *************

```
RTC
     7    6    5    4    3    2    1    0

     -    -    -    -    -    -    -    -
     ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
     +----+----+----+----+----+----+----+-------- DATDT
```

Note : Date data to the calendar clock
Write 07H into 11B4H befor access Date data to the calender clock.

*** I/O address 11B5H (Read)(Write) Month Data *************

```
RTC
     7    6    5    4    3    2    1    0

     -    -    -    -    -    -    -    -
     ¦    ¦    ¦    ¦    ¦    ¦    ¦    ¦
     +----+----+----+----+----+----+----+----------- METDT
```

Note : Month data to the calendar clock
Write 08H into 11B4H befor access Month data to the calender clock.

```
*** I/O address    11B5H (Read)(Write)    Year Data ************

RTC
    7     6     5     4     3     2     1     0

    -     -     -     -     -     -     -     -
    |     |     |     |     |     |     |     |
    +-----+-----+-----+-----+-----+-----+-----+--------- YERDT
```

Note : Year data to the calendar clock
Write 09H into 11B4H befor access Year data to the calender clock.

```
*** I/O address   11B5H (Read)(Write)   Control Register A ********

RTC
    7      6       5       4       3       2       1       0

   UPD  DVSEL2  DVSEL1  DVSEL0  SQSEL3  SQSEL2  SQSEL1  SQSEL0
    |      |       |       |       |       |       |       |
    |      +-------+-------+       +-------+-------+-------+
    |                      |                               |
    |                      |                     Rate selection of SQW
    |                      +-------------------- Divider selection
    |                                            (should set '0,1,0')
    +------------------------------------------- Update in progress
```

Note :
Write 0AH into 11B4H befor access the control register A.

```
*** I/O address   11B5H (Read)(Write)   Control Register B *******

RTC
  7    6   5   4    3     2     1    0

UPDDS PIE AIE UEI SQWEN DTMOD H2412 DSE
  |    |   |   |    |     |     |    |
  |    |   |   |    |     |     |    +- Daylight Saving Enable
  |    |   |   |    |     |     +------ 0:12h mode, 1:24h mode
  |    |   |   |    |     +------------ Data Mode 1:binary, 0:BCD
  |    |   |   |    +------------------ Square Wave Enable
  |    |   |   +----------------------- Update Ended Interrupt
  |    |   +--------------------------- Alarm Interrupt Enable
  |    +------------------------------- Periodic Interrupt Enable
  +------------------------------------ Disable update sequence
```

Note:
Write 0BH into 11B4H befor access the control register B.

```
*** I/O address  11B5H (Read)(Write)   Control Register C *****

RTC
 7      6     5     4     3     2     1     0

INTRQ  PIF   AIF   UIF    -     -     -     -
  |     |     |     |     |     |     |     |
  |     |     |     |     |     |     |     |
  |     |     |     |     +-----+-----+-----+---- Don't care
  |     |     |     +---------------------------- Update Interrupt Flag
  |     |     +---------------------------------- Ararm Interrupt Flag
  |     +---------------------------------------- Periodic Interrupt Flag
  +---------------------------------------------- Interrupt Request Flag

 Note: Address 11B4H : Write data 0CH
Write 0CH into 11B4H befor access the control register C.
```

```
*** I/O address  11B5H (Read)    Control Register D ***********

RTC
     7     6     5     4     3     2     1     0

   RAMVD   -     -     -     -     -     -     -
     |     |     |     |     |     |     |     |
     |     +-----+-----+-----+-----+-----+-----+----- Don't care
     +----------------------------------------------- RAM Valid Flag

 Note: Address 11B4H : Write data 0DH
Write 0DH into 11B4H befor access the control register D.
```

```
*** I/O address   11B6H (Read)    DIP SW. #2 ******************

 7    6    5    4    3    2    1    0

SW16 SW15 SW14 SW13 SW12 SW11 SW10 SW9
 |    |    |    |    |    |    |    |
 |    |    |    |    |    |    |    |
 |    |    |    |    |    |    |   SW 9.. Country Select 0
 |    |    |    |    |    |    +-- SW10.. Country Select 1
 |    |    |    |    |    +------- SW11.. Country Select 2
 |    |    |    |    +------------ SW12.. Country Select 3
 |    |    |    +----------------- SW13.. Parity Check Enable
 |    |    +---------------------- SW14.. Video Enable
 |    +--------------------------- SW15.. ASYNC Primary/Secondary
 +-------------------------------- SW16.. ASYNC Enable
```

```
*** I/O address  11B7H (Write)   Clock Speed Register **********

CLOCK & WAIT
  7     6    5    4    3     2     1     0

 CLKSP  -    -    -    -    W2    W1    W0
   |                         |     |     |
   |                         +-----+-----+
   |                               |
   |                         Write state insertion
   |                         000 --> 0 wait : 111 --> 7 waits
   +---------------------------- 0:4.77 MHz 1:7.16 MHz
```

```
*** I/O address  11B8H (Read)   Power ON Status Register ********

   7     6     5     4     3     2     1     0

   -     -     -     -     -   PWSW ALARM MODON
                                |     |     |
                                |     |     +----- 1: Modem on
                                |     +---------- 1: Time alarm on
                                +--------------- 0: Power SW on
```

```
***  I/O address   11B8H (Write)   Power Off Signal ************

  7      6       5         4          3    2    1    0
 PWOFF  SWFFS  MODEMEN  MODEMWR       -    -    -    -
  |      |       |         |
  |      |       |         +-------------------- Modem Enable Write
  |      |       +------------------------------ Modem Wake up Enable
  |      +-------------------------------------- Power SW FF Set
  +--------------------------------------------- Power Off
```

```
*** I/O address   11B9H (Write)  Peripheral Select Register ****

    7       6       5    4    3    2    1    0

 SELASY SELPRM      -    -    -    -    -    -
    |       |
    |       +-------- ASYNC 0: Primary 1: Secondary
    +--------------- Internal ASYNC 0: Enable 1: Disable
```

```
*** I/O address  11BAH (Read)(Write)  FD Mode Register ********

   7        6     5     4     3     2     1     0

FDMODE   ASPD   BSPD  DCGA  DCGB    -     -     -
  |        |     |     |     |
  |        |     |     |     |
  |        |     |     |   1: When unloded the diskette from
  |        |     |     |      the drive B,this bit will be 1
  |        |     |     |   0:                not unloaded     (red)
  |        |     |     +-- 1: When unloaded the diskette from
  |        |     |            the drive A,this bit will be 1
  |        |     |         0:                not unloaded      (read)
  |        |     +-------- B drv speed 1:360rpm 0:300rpm
  |        +-------------- A drv speed 1:360rpm 0:300rpm
  +----------------------- 1:Standard 0:Mini
```

```
*** I/O address  11BCH (Read)  Interrupt Request Register ******

INTERRUPT #2
   7    6    5    4     3      2     1    0

   -    -    -    -   IRR11    -   IRR9 IRR8
   |    |    |    |     |      |     |    |
   +----+----+----+     |      |     |    |
                  |     |      |     |  In service bit of option
                  |     |      |     +-- In service bit of option
                  |     |      +------ (not used)
                  |     +----------- In service bit of power sw. off
                  +---------------- Don't care
```

Note: Before accessing this register, you should write OCW3 command onto 11BCH.

```
*** I/O address  11BCH (Read)   In Service Register ***********

INTERRUPT #2
   7     6     5     4      3       2      1     0

   -     -     -     -    ISR11     -    ISR9  ISR8
   |     |     |     |      |       |      |     |
   +-----+-----+-----+      |       |      |     |
                     |      |       |      |  In service bit of option
                     |      |       |      +-- In service bit of option
                     |      |       +------- (not used)
                     |      +------------- In service bit of power sw.
                     +------------------- Don't care                off
```

Note: Before accessing this register, you should write OCW3 command onto 11BCH.

```
*** I/O address    11BCH (Write)        OCW2 *******************

INTERRUPT #2
   7   6     5      4    3     2      1      0

   -  SEOI  NEOI    0    0   INTLV2 INTRV1 IMTRV0
   |   |     |                 |      |      |
   |   |     |                 +------+------+-- Intr. level
   |   |     +---------------------------------- Normal EOI Mode
   |   +---------------------------------------- Special EOI Mode
   +-------------------------------------------- Don't care
```

```
*** I/O address    11BCH (Write)        OCW3  ******************

INTERRUPT #2
   7    6    5    4    3    2    1    0

   -    -    -    0    1    -   RRB  ISIR
   |    |    |              |    |    |
   +----+----+              |    |    |
             |              |    |    |
             |              |    |   0:Interupt Request Register
             |              |    |   1:In-Service Register
             |              |    |   X:If bitl = 0
             |              |    +-- Read register
             |              |         0:Disable, 1:Enable
             +--------------+------- Don't care
```

```
*** I/O address 11BDH (Read)(Write)  Interrupt Mask Register ***

INTERRUPT #2
     7    6    5    4    3    2    1    0

     -    -    -    -  IMB11  -  IMB9  IMB8
     |    |    |    |         |
     +----+----+----+---------+------------- Don't care
```

Note : Interrupt Mask Bit
1: Set Mask
0: Clear Mask

```
*** I/O address    11BEH (Read)    Select Reg. ****************

INTERRUPT
  7    6    5    4    3    2        1     0

  -    -    -    -    -  SELSTL  SELSTH   -
  ¦    ¦    ¦    ¦    ¦    ¦        ¦     ¦
  +----+----+----+----+    ¦        ¦     +- Don't care
                      ¦    ¦        +-------- Select 20H status reg.
                      ¦    ¦                   0:IRR 1:ISR
                      ¦    +----------------- Select 11BCH status reg.
                      ¦                        0:IRR 1:ISR
                      +---------------------- Don't care
```

7.5 GATE ARRAY AND IC DESCRIPTIONS

GAMYMC

The GAMYMC has the following functions.

1. Memory control
   The GAMYMC generates the $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals of the DRAM and refreshes the DRAM.
   It also generales the access signal for the ROM.

2. CPU clock change
   The CPU clock is changed from 4.77MHz to 7.16MHz, or vice versa.

3. Wait control
   Wait cycles 0 through 7 to the VRAM or ROM are inserted by software.

4. Parity check.

5. NMI circuit control.

6. Reset circuit control.

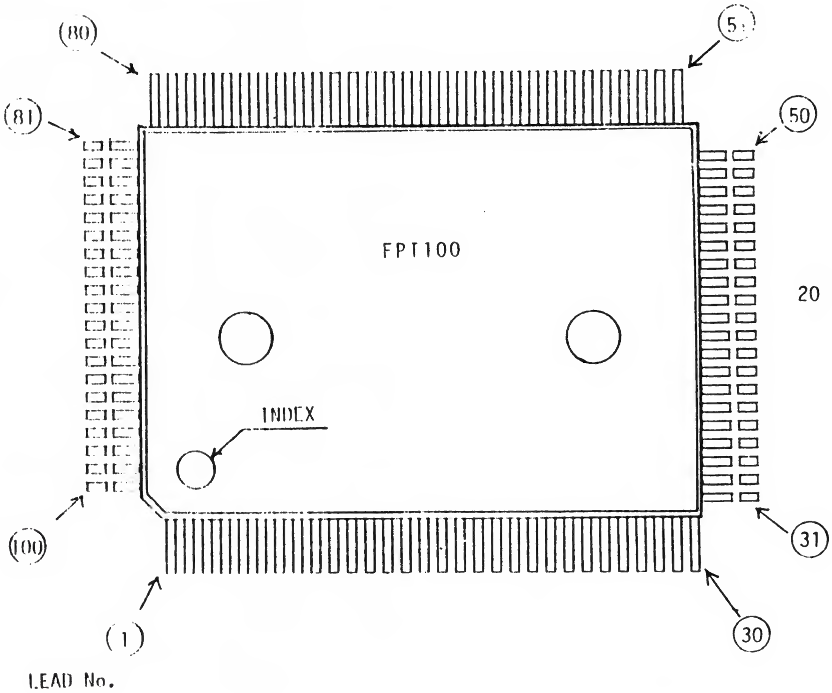

FIGURE 7-15. GAMYMC PIN DIAGRAM

TABLE 7-19. GAMYMC PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AD15-AD8	62-64,66-70	I	CPU address data bus 15-8.
AD7-AD0	71-77	I/O	CPU address data bus 7-0.
A19-A16	58-61	I	CPU address bus 19-16.
$\overline{BHE}$	52	I	Bus high enable signal.
$\overline{S2}$-$\overline{S0}$	57-55	I	CPU status signal.
C14M	81	I	14.31818MHz clock.
CLK0	99	O	CPU clock divides C14M into two or three pulses. (7.159MHz or 4.773MHz)
C4P7	83	O	4.773MHz clock. Synchronous with the CLK 0 clock.
CLK	100	I	CPU clock
RDY4-RDY1	50-57	I	Ready input. When one of these signals is low, the RDY0 terminal is low.
RDY	46	O	Ready output. This signal is connected to the CPU RDY signal input terminal.
ARDY	87	O	Not used in this system.
$\overline{PSSW}$	41	I	Reset switch input
$\overline{RSPD}$	89	I	Power down signal
RESO	96	O	Power down signal. When the $\overline{RSSW}$ or the $\overline{RSPD}$ signal is low, the RESO signal becomes high.
$\overline{RESN}$	97	O	Reset signal. When the RSSW or the $\overline{RSPD}$ signal is low, the RESN signal becomes low.
NMI	45	O	Non-maskable interrupt. This signal is generated under the following conditions. (1) Memory parity error (2) Interrupt from the 8087 (3) Parity error signal from the option slot.
DMA	43	I	Indicates the DMA operation. "H" : DMA operation "L" : CPU access
NPI	44	I	Interrupt request signal from the co-processor 8087.
$\overline{IOPR}$	85	I	Parity error signal from the option slot
SPK	27	I	Speaker signal
TC2	26	I	Timer signal
TEST	16	I	Test terminal. Should be low in use.
S	17	I	Test signal Should be low in use.
HSPD	91	O	High speed clock mode. "L" : 4.77MHz "H" : 7.16MHz

$\overline{\text{PROM}}$	86	O	When reading memory address "F0000H-FFFFFH", this signal becomes low.
$\overline{\text{WRBF}}$	93	O	Not used in this system.
SW8-SW1	38-31	I	Input terminal of the DIP SW status. SW ON : "low" SW OFF: "high"
MA8-MA0	18,14-7	O	Mulitiplexed DRAM address.
MDPH	23	I/O	DRAM parity bit. High byte to odd address.
MDPL	22	I/O	DRAM parity bit. Low byte to even address.
$\overline{\text{RAS3}}$	6	O	Row address strobe. RAS signal for the upper byte (odd address) of the 512KB RAM or the main control board.
$\overline{\text{RAS2}}$	5	O	Row address strobe. RAS signal for the lower byte (ever address) of the 512KB RAM on the main control board.
$\overline{\text{RAS1}}$	21	O	Row address strobe. RAS signal for the upper byte (odd address) of the 128KB RAM on the memory slot.
$\overline{\text{RAS0}}$	20	O	Row address strobe. RAS signal for the lower byte (even address) of the 128KB RAM on the memory slot.
$\overline{\text{CAS}}$	2	O	Column address strobe signal.
$\overline{\text{WE}}$	1	O	Write enable signal.

GAMYVA

The GAMYVA (combined with the GAMYVD) provides the video control circuit. The GAMYVA employs the address control and converts 8 bits of the GDC89322 to/from 16 bits of the system bus.

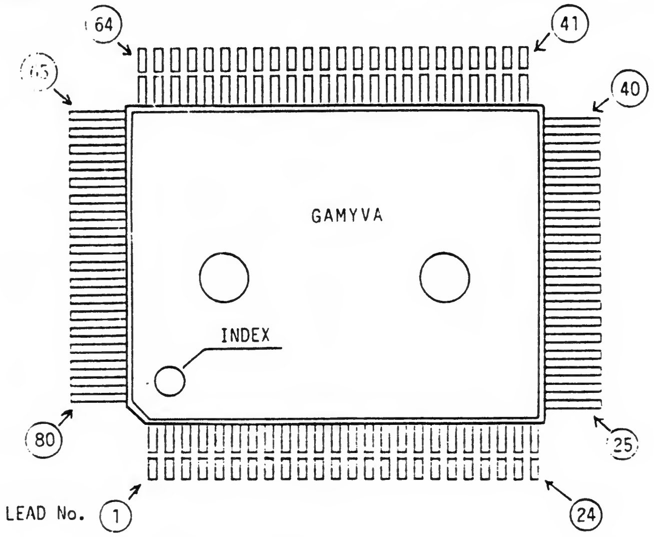

FIGURE 7-16. GAMYVA PIN DIAGRAM

TABLE 7-20. GAMYVA PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AD15-AD18	18-13,10,9	I/O	CPU address data bus
AD7-AD0	7-0	I	CPU address data bus
$\overline{\text{S2}}$-$\overline{\text{S0}}$	24,22,21	I	CPU Status lines
$\overline{\text{BHE}}$	20	I	Indicates that the upper address (AD15-AD8) is valid.
C16M	42	I	Dot clock for the monochrome monitor.
C14M	72	I	Dot clock for the color monitor.
C8M	25	I	CPU system clock.
$\overline{\text{RSET}}$	11	I	When the $\overline{\text{RSET}}$ signal is input, registers in the GAMYVA are initialized.
MALT	77	I	Latches the memory address (MA12-0) and the raster address (RA1-0) from the CRTC.
$\overline{\text{CPSL}}$	80	I	When the CPU controls the VRAM, the $\overline{\text{CPSL}}$ signal changes the VRAM address (VA7-0)
MPX	78	I	Exchange signal of the row address and the column address of the VRAM.

IDCK	75	I	Input terminal of the dot clock.
CGSL	60	I	The jumper setting of the font selection for the character generator is input to this terminal.
MA12-MA0	29,31,34,36 38,40,57,55 53,49-46	I	Memory address from the CRTC.
RA1-RA0	45,44	I	Raster address from the CRTC.
TEST	43	I	Test terminal for the GAMYVA. Should be pulled down in use.
GD7-GD0	32,35,37,39 58,56,54,50	I/O	Internal register data bus of the CRTC.
VA7-VA0	69-64,62,61	O	VRAM address
$\overline{CS}$	30	O	When reading/writing the internal register of the CRTC, this signal becomes low.
RS	28	O	Internal register select signal for the CRTC. "L" : Address register "H" : Internal register
$\overline{WR}$	26	O	Write signal for the internal register of the CRTC.
$\overline{RD}$	27	O	Read signal for the internal register of the CRTC.
$\overline{WAIT}$	19	O	Wait request signal for the CPU. This signal generates the CPU ready signal by adjusting with the GAMYMC.
$\overline{HSEL}$	79	O	This signal indicates which address (upper or lower) accesses to the VRAM. "L" : Lower address "H" : Upper address
MONI	70	O	Not used in this system.
DCLK	74	O	Dot clock. In monochrome mode, the C14M clock is output. In color mode, the C16M clock is output from this terminal.

GAMYVD

The GAMYVD employs the video RAM and outputs the video signal.

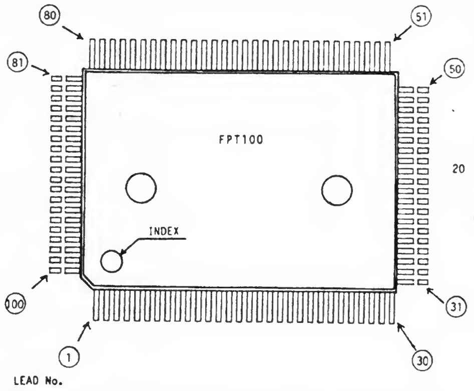

FIGURE 7-17. GAMYVD PIN DIAGRAM

TABLE 7-21. GAMYVD PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AD15-AD0	8-13,16-25	I/O	CPU address data bus.
A19-A16	96-99	I	CPU address bus.
$\overline{S2}$-$\overline{S0}$	2,4,5	I	CPU status line.
$\overline{BHE}$	6	I	Indicates that the upper address (AD15-AD8) is valid.
C8M	1	I	CPU system clock.
$\overline{RSET}$	14	I	When the $\overline{RSET}$ signal is input, registers in the GAMYVD are initialized.
$\overline{WAIT}$	7	O	Wait request signal for the CPU. This signal generates the CPU ready signal by adjusting timing with the GAMYMC.
DCLK	31	I	Dot clock for the video signal. Color mode : 14.31818 MHz Monochrome mode : 16.00 MHz
$\overline{MVAS}$	100	O	Indicates that the video is active.
GD7-CGD0	87-95	I	Data input for the character generator.
CA12-CA3	76-86	O	Data input for the character generater.
VD15-VD0	64-48	I/O	VRAM data bus.
$\overline{RAS}$	66	O	$\overline{RAS}$ signal for the VRAM.
$\overline{CASH}$	46	O	$\overline{CAS}$ signal for the upper address of the VRAM area. (B8000H-BFFFFH).

$\overline{\text{CASL}}$	47	O	$\overline{\text{CAS}}$ signal for the lower address of the VRAM area. (B0000-B7FFFH)
$\overline{\text{WEH1}}$	43	O	Write enable signal for the VRAM (Upper,VD15-VD8)
$\overline{\text{WEL1}}$	45	O	Write enable signal for the VRAM (Lower, VD15-VD8)
$\overline{\text{WEH0}}$	42	O	Write enable signal for the VRAM (Upper, VD7-VD0)
$\overline{\text{WEL0}}$	44	O	Write enable signal for the VRAM (Lower, VD7-VD0)
RA3-RA0	36-39	I	Raster address output from the CRTC.
CCLK	41	O	Display timing signal of the CRTC. During the display, this signal becomes high.
CUDS	34	I	Cursor display signal of the CRTC. This signal becomes high.
VSYN	33	I	Vertical synchronous signal of the CRTC.
HSYN	32	I	Horizontal synchronous signal of the CRTC.
I	68	O	Intensity signal.
R	69	O	Red video signal.
G	70	O	Green video signal.
B	71	O	Blue video signal.
H	73	O	Horizontal synchronous signal.
V	72	O	Vertical synchronous signal. Color mode: Positive Monochrome mode: Negative
CMCL	75	O	Composit video signal in color mode.
CMBL	74	O	Composit video signal in color mode.
MALT	30	O	Latches the CRTC address (MA13-MA0) for the CRTC.
MPX	29	O	Multiplex signal for row address and column address.
CSEL	26	O	Indicates that the CPU controls VRAM.
$\overline{\text{HSEL}}$	27	I	This signal indicates which address (upper or lower address) accesses to the VRAM. "L" : Lower address "H" : Upper address
TEST	67	I	Test terminal for the gate array. Should be pulled down in use.

GAMYIO

The GAMYIO has the following functions.

1. Interrupt controller.
2. RS-232C interface.
3. FDD interface.
4. Printer interface.
5. Speaker interface.
6. Address decoder.

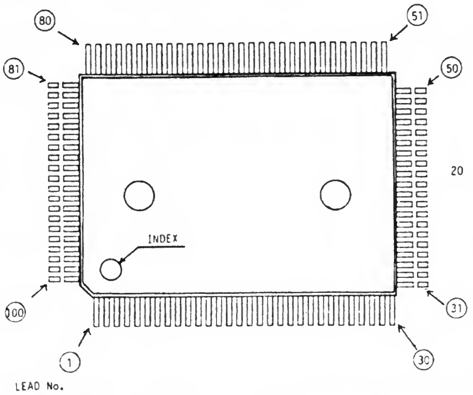

FIGURE 7-18. GAMYIO PIN DIAGRAM

TABLE 7-22. GAMYIO PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
REST	14	I	System reset.
CLK	50	I	System clock.
AEN	48	I	Address enable signal in DMA mode
$\overline{\text{A11B}}$	44	I	When this signal is low, I/O address 11B0H-11BFH is selected.
$\overline{\text{A9X}}$-$\overline{\text{A1X}}$,$\overline{\text{A0}}$	18-27	I	Address bus.
$\overline{\text{IOR}}$	2	I	I/O read signal.
$\overline{\text{IOW}}$	1	I	I/O write signal.
IOWN	46	I	I/O write signal. When this signal is active, the write data must be definite.
JUMP	30	I	Changes the printer interface address. "L" : 378H - 37AH "H" : 3BCH - 3BEH
BUSY	94	I	Busy signal of the printer.
$\overline{\text{ACK}}$	95	I	Acknowledge signal of the printer.
$\overline{\text{PE}}$	93	I	Paper empty signal of the printer.
SLCI	92	I	Input signal for the printer selection.
$\overline{\text{ERRO}}$	98	I	Error signal of the printer.
$\overline{\text{INTA}}$	45	I	Interrupt acknowledge signal of the CPU.
IRTM	11	I	Interrupt request signal from the timer.

IRK1	47	I	Interrupt request signal from the keyboard.
IR2	5	I	Interrupt request signal from the option slot.
IR3	10	I	Interrupt request signal from the option slot.
IR4	9	I	Interrupt request signal from the option slot.
IR5	8	I	Interrupt request signal from the option slot.
IR6	76	I	Interrupt request signal from the FDD.
IR8	7	I	Interrupt request signal from the option slot.
IR9	6	I	Interrupt request signal from the option slot.
IRK2	13	I	Not used in this system.
IRPW	4	I	Interrupt request signal from the power SW.
TES0	16	I	Test terminal for the gate array.
TES1	51	I	Test terminal for the gate array.
C3P6	91	I	Transmit clock for the RS-232C.
BAIN	80	I	Baud rate clock input terminal.
SIN	86	I	Serial data input of the RS-232C.
RI	82	I	Ring indicator of the RS-232C.
CTS	89	I	Data set ready of the RS-232C.
RLSD	87	I	Carrier detect of the RS-232C.
CHDA	74	I	Disk drive change signal for the FDD-A
CHDB	73	I	Disk drive change signal for the FDD-B
C16M	52	I	Input terminal for the FDD interface (16MHz)
PS0,PS1	59,58	I	These signals adjust the timing of write data to get a read margin in the MFM mode.
WRGA	56	I	FDD write enable signal.
WOAI	57	I	FDD write data.
$\overline{GBF}$	39	0	Buffer enable signal. When reading the internal register, 8253, and the status of the DIP SW, this signal becomes low.
$\overline{TCS}$	42	0	Chip select signal for the 8253.
SPKD	17	0	Speaker data.
TGA2	43	0	Speaker data gate
$\overline{SLCO}$	96	0	Select-in signal for the printer.
$\overline{INIT}$	97	0	Initialize signal for the printer.
$\overline{AUTO}$	99	0	Auto-feed-XT signal for the printer.
$\overline{STRB}$	100	0	Data strobe signal for the printer
$\overline{CNTW}$	41	0	Output terminal of the write pulse for the printer.

$\overline{\text{DPSW}}$	29	O	Read pulse for the DIP SW status.
INTR	54	O	Interrupt request signal for the CPU.
$\overline{\text{BAOT}}$	79	O	Output terminal for the baud rate generator.
SOUT	83	O	Serial data output at the RS-232C.
$\overline{\text{RTS}}$	84	O	$\overline{\text{RTS}}$ (Reqest to send) signal of the RS-232C.
$\overline{\text{DTR}}$	85	O	$\overline{\text{DTR}}$ (Data terminal ready) signal at the RS-232C.
$\overline{\text{CSFD}}$	60	O	Chip select signal for the FDC 765.
$\overline{\text{W3F2}}$	81	O	Write pulse for the digital output register. (Not used in this system.)
FDCK	55	O	Clock for the 765.
DRQC	64	O	Sampling clock for the DMA request signal of the 765.
WCLK	77	O	Write clock of the 765.
WDAO	61	O	Write data of the FDD.
MTB	67	O	Motor on signal for the drive B, C and D.
MTA	68	O	Motor on signal for the drive A.
$\overline{\text{DMAG}}$	49	O	DMA enable signal for the FDD.
RSTF	66	O	Reset signal of the 765.
DS3	72	O	Selection signal of the drive D.
DS2	69	O	Selection signal of the drive C.
DS1	70	O	Selection signal of the drive B.
DSO	71	O	Selection signal of the drive A.
MIN	62	O	FDD mode selection signal "L" : standard "H" : mini
ASPD	63	O	Motor speed selection signal of drives A and B.
BSPD	75		"L" : 360 rpm "H" : 300 rpm
D7X-DOX	38-31	I/O	Data bus.

GAMYDM

The GAMYDM is used for the DMA control. The GAMYDM employs the interface between the 8237 and the system bus.The GAMYDM changes the $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOW}$ and $\overline{IOR}$ signal of the 8237 to the status signal $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$ for the CPU and changes the HRO, HLDA signals of the 8237 to the $\overline{RO/OT}$ signal for the CPU. The page register of the DMA is included in the GAMYDM.

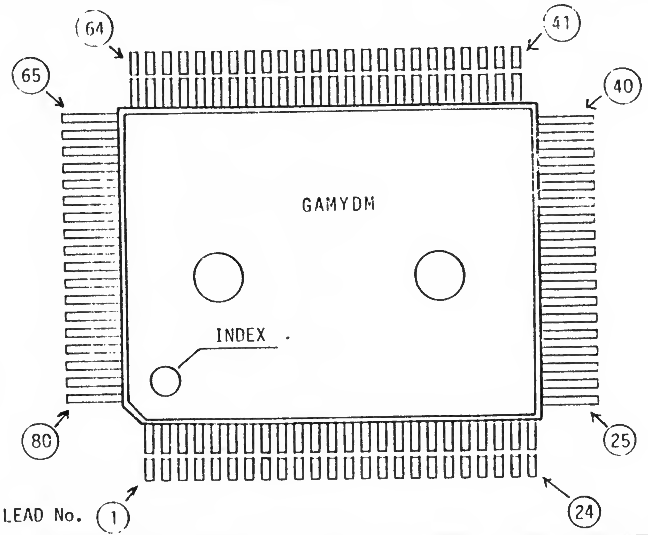

FIGURE 7-19. GAMYDM PIN DIAGRAM

TABLE 7-23. GAMYDM PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
RDYI	27	I	Ready from GAMYMC (memory control gate array)
$\overline{IOR}$	31	O	This pin is only active in DMA operation to notify I/O devices to output read data.
$\overline{IOW}$	32	O	This pin is only active in DMA operation to notify I/O devices to input write data.
$\overline{S2}$-$\overline{S0}$	28,29,30	I/O	Status inputs when the 8237 is programmed to set parameters. During DMA operation, these pins output status.
CLK	25	I	Clock input. 4.77MHz clock in IBM mode. 7.16MHz clock in native mode.
A19-A16	10,8,6,4		High-Z except for DMA mode. During DMA operation, these pins output memory address 19-16.
AD15-AD0	1,3,5,7,9,11	I/O	Except in DMA operation, they are address 14,15,16,17, and data inputs and used to program DAMC 18,19,20,21, 8237. During DMA they output memory 22,24 address 0-15.

$\overline{\text{BHE}}$	13	I/O	Except in DMA operation, this is a bus high enable input. During DMA operation, this outputs a bus high enable signal.
$\overline{\text{RQGT}}$	80	I/O	This pin issues REQUEST pulse when 8237 activates its HRQ pin, then it is set as an input immediately to receive an acknowlage pulse from V30 CPU. After receiving ACK, it is provided as an output and issues release pulse when 8237 disables its a HRQ pin to notify CPU to terminate "bus hold operation".
RST	41	I	This signal initializes all the internal registers, F.F.S and latches.
$\overline{\text{DIOR}}$	65		This pin is connected to 8237's $\overline{\text{IOR}}$ pin and used to read 8237's internal registers.
$\overline{\text{DIOW}}$	67		This pin is connected to 8237's $\overline{\text{IOW}}$ pin and used to write data into 8237's internal registers.
RDYO	62	O	Each signal DMA transfer is extended as I/O devices need longer access time. (This pin is connected to 8237's ready pin)
$\overline{\text{MR}}$	69	I	During DMA operation, it receives memory write timing signal from 8237. It is inactive except in DMA period.
$\overline{\text{MW}}$	71	I	During DMA operation, it receives memory write-timing signal from 8237. It is inactive except in DMA period.
$\overline{\text{CS37}}$	66,68,70,72	O	Chip select for 8237 DMAC.
A7-A4	54	O	These signal accept the four most significant addresses from 8237 during DMA service. Always low level except in DMA period. (DMA address 3-0)
A3-A0	69,61,59,57	I/O	In programming mode, they issue addresses to select internal registers. During DMA service, they accept DMA addresses from 8237.(DMA address 3-0)
ADS B	58	I	Address strobe is used to strobe the upper address byte into a latch. (DB7-8)
AEN	56	I	Address enable for DMA address on the system bus.
DB7-DB0	37,38,39,40 46,47,48,49	I	The data bus lines are bidirectional three-state signals connected to the 8237's data bus. In the programming condition they receive and send read/write data. During DMA cycles the most significant 8-bit address is input from 8237. (DMA address 15-8)
HRQ	55	I	Input from 8237 hold request. After the rising edge of HRQ, GAMYDM issues a request pulse from its $\overline{\text{RQGT}}$ pin to V30. After 8237 inactivates its HRQ signal, a release pulse is issued from this pin.

HLDA	60	O	Hold acknowledge activates 8237's HLDA pin after V30 issues an acknowledge pulse.
DMCK	53	O	8237 clock is also provided to this pin. C470 pin is usually connected to the DMCK.(DMA clock)
$\overline{\text{DAK3-1}}$	44,45,43	I	DMA acknowledge is used in the GAMYDM decode from which the DMA channel should be selected. A DMA page register corresponding to each DMA channel is selected by software proceeding the DMA operation.
C47I	34	I	A 4.77MHz clock is provided by memory control gate array to generate C470 which satisfies MIN. and MAX. clock requirement of 8237.
C470	51	O	4.77MHz clock output provides for the DMCK pin and 8237 clock.
EALW	75	O	This pin goes high when the early write (extended write) selection is programmed.
VDD	33,73	-	Ground.
VSS	2,12,23,42 52,63	-	+5V.

GAMYOS

The GAMYOS has the following functions:

(1) Address latch, address decode.
(2) Selection of the system clock.
(3) Conversion of the data bits (16 or 8 bits)
(4) Wait control
(5) Keyboard interface
(6) RTC control
(7) Power control
(8) Generation of the control signal
(9) Generation of the timer clock
(10) DMA control

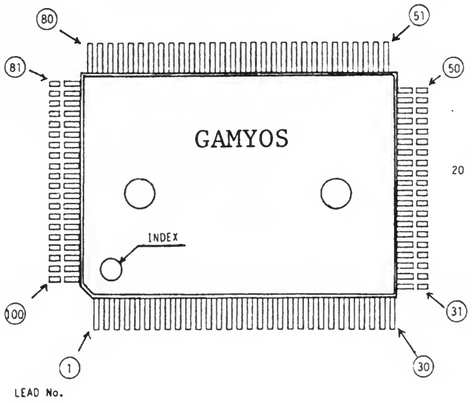

FIGURE 7-20. GAMYOS PIN DIAGRAM

TABLE 7-24. GAMYOS PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
A19C-A16C	23-20	I	Address status line.
AD15-AD0	19-1	I/O	Address data bus.
$\overline{\text{S2}}$-$\overline{\text{S0}}$	27-25	I	CPU status line.
$\overline{\text{BHE}}$	24	I	CPU bus high enable/status.
ALE	80	O	Address latch strobe.
ALEO	89	O	ALE signal for the option slot.
DA7-DA0	70-77	I/O	8-bit data bus.
$\overline{\text{IOW}}$	87	O	I/O write strobe signal.
$\overline{\text{IOR}}$	86	O	I/O read strobe signal.
$\overline{\text{MEMW}}$	85	O	Memory write strobe signal.
$\overline{\text{MEMR}}$		O	Memory read strobe signal.
$\overline{\text{INTA}}$	69	O	Interrupt acknowledge signal.
IOWN	68	O	I/O write strobe signal for latch.
$\overline{\text{DIR}}$	61	O	Direction signal of the data buffer "L" : data input
$\overline{\text{GBF}}$	62	O	Chip enable signal of the data buffer.
A11B	67	O	Address decoded signal. Used for the original I/O port of this system.

A19-A17	81-83	O	Address signal 19-17
A0	84	O	Address signal 0.
IORY	34	I	Ready signal for the 8 bit system of the option slot.
RDYS	33	O	Ready output signal.
TEST	48		Output terminal of the test for the GAMYOS.
RTAL	95	O	Address strobe of the RTC.
$\overline{RTDR}$	96	O	Data read strobe of the RTC.
$\overline{RTDW}$	97	O	Data write strobe of the RTC.
PWWE	94	O	Write strobe for the power control port.
PW7-PW0	56-90,91-93	O	Input bus of the I/O port 11B8H.
$\overline{CSVD}$	51	I	Becomes high impedance of AD15-AD0 in read cycle.
$\overline{CSKJ}$	52	I	Becomes high impedance of AD15-AD0 in read cycle.
CLK	100	I	System clock 4.77MHz or 7.16MHz.
AEN	35	I	Address enable signal of the 8237 in DMA mode.
$\overline{DIOW}$	37	I	I/O write status in DMA mode.
$\overline{DIOR}$	36	I	I/O read status in DMA mode.
KCKI	41	I	Keyboard clock.
$\overline{KDAI}$	43	I	Keyboard scan code.
$\overline{KCNI}$	45	I	Keyboard stop signal.
$\overline{KCKO}$	42	O	Keyboard initialization signal.
KDAO	44	O	Keyboard interrupt data line control.
$\overline{KCNO}$	46	O	Keyboard buffer bit (MSB).
REST	30	I	System reset.
C47M	31	I	4.77MHz clock.
COMP	98	I	Mode set terminal for the control signal to the clock synchronized to the C47M clock.
C0	49	I	Clock input terminal.
C1	50	O	Output terminal where the CD clock is divided into two.
INVI	38	I	Inverter input.
INVO	39	O	Inverter output.
TCLK	64	O	Output; terminal of the clock for time divided C47M clock into four.

uPD70116/V30

Figure 7-21 shows the uPD70116V30 pin diagram, and Table 7-25 lists the pin descriptions for this IC.

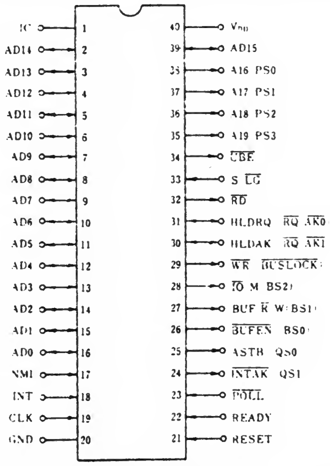

FIGURE 7-21, uPD701161V30 PIN DIAGRAM

TABLE 7-25. uPD701161V30 PIN DESCRIPTION

PIN NO.	SIGNAL NAME	I/O	NAME AND FUNCTION
9-16	AD7-AD0	I/O	Address Data Bus: These lines constitute the time multiplexed memory/IO address (T1)and data (T2,T3,Tw and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local.
2-8,39	A15-A8	O	Address Bus: These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".
34	$\overline{UBE}$	O	Upper Byte Enable: During bus cycle T2-T4, this signal indicates that AD15-AD8 are active.
35-38	PS3-PS0	O	During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw and T4. PS3 is always low. The status of the interrupt enable flag bit (PS2) is updated at each clock cycle. PS1 and PS0 are encoded as shown below. The information indicates which segment register

			is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge"
32	$\overline{\text{RD}}$	O	Read: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of BSC. This signal is used to read devices which reside on the CPU local bus. RD is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the CPU local bus has floated. This signal floats to 3-state OFF on "hold acknowledge".
22	READY	I	Ready: is the acknowledgement from the address memory or I/O device that it will complete the data transfer. The RDY signal from the memory or I/O is synchronized by the GAMYMC clock generator to/from READY. The signal is active HIGH. The CPU READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.
18	INT	I	Interrupt Request: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored via an interrupt vector look-up table located in system memory. It can be internally masked by software, resetting the interrupt enable bit. INT is internally synchronized. This signal is active HIGH.
23	$\overline{\text{POLL}}$	I	Not used in the system.
17	NMI	I	Non-Maskable Interrupt: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored via an interrupt verctor look-up table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET	I	Reset: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
19	CLK	I	Clock: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.

30,31	$\overline{RQ}/\overline{AK0}$ $\overline{RQ}/\overline{AK1}$	I/O	Request/Grant: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with RQ/AK0, having higher priority than RQ/AK1. RQ/AK has an internal pull-up register, so may be left unconnceted. The request/grant sequence is as follows: 1.A pulse of one CLK width from another local bus master indicates a local bus request "hold" to the CPU(pulse 1). 2.During a T4 or T1 clock cycle, a pulse one clock wide from the CPU to the requesting master (pulse 2) indicates that the CPU has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3.A pulse one CLK wide from the requesting master indicates to the CPU (pulse 3) that the "hold" request is about to end and that the CPU can reclaim the local bus at the next CLK. The CPU then enters T4. Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is mode, the two possible events will follow: 1. The local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. The four rules for a currently active memory cycle apply when condition number 1 is already satisfied.

33	$S/\overline{LG}$	I	Small/Large: indicates the mode in which the processor is to operate.
26-28	BS2,BS1,BS0	O	Status: is active during clock high of T4, T1, and T2, and is returned to the passive state(1,1,1)during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by BS2, BS1, or BS0 during T4 cycle is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they floar to 3-state OFF.
24,25	QS1,QS0	O	Queue Status: provides status to allow external tracking of the internal CPU instruction queue. The queue status is valid during the CLK cycle, after which the queue operation is performed.

8087

Figure 7-22 shows the 8087 pin diagram; Table 7-26 lists the 8087 pin descriptions.

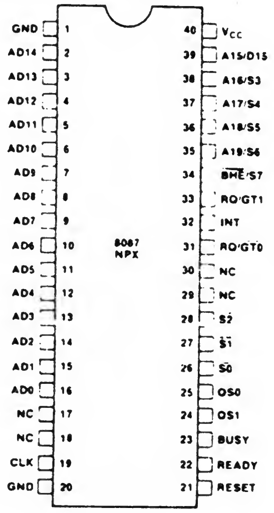

FIGURE 7-22. 8087 PIN DIAGRAM

TABLE 7-26. 8087 PIN DESCRIPTION

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AD15-AD0	16-2	I/O	Address data: These lines constitute the time multiplexed memory address (T1) and data (T2,T3,Tw,T4) bus. A0 is analogous to BHE for the lower byte data bus, pins D7-D0. It is LOW during T1 when a byte is transferred on the lower portion of the bus in memory operations. Eight-bit oriented devices tied to the lower half of the bus normally use A0 to condition chip select functions. These lines are
Vcc	40	-	Power: Vcc is the +5V power supply pin.
GND	20	-	Ground: GND are the ground pins.

A19/S6,	35	I/O	Address memory: During T1 these are the four most significant address lines for memory operations. During memory operations, status information is available on these lines during T2,T3, Tw and T4. For 8087 controlled bus cycles, S6, S4 and S3 are reserved and currently one (HIGH), while S5 is always LOW. These lines are inputs which the 8087 monitors when the 8086/8088 is in control of the bus.
A18/S5,	36	I/O	
A17/S4,	37	I/O	
A16/S3	38	I/O	
$\overline{\text{BHE}}$/S7	34	I/O	Bus high enable: During T1 the bus high enable signal ($\overline{\text{BHE}}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight-bit oriented devices tied to the upper half of the bus normally use $\overline{\text{BHE}}$ to condition chip select functions. $\overline{\text{BHE}}$ is LOW during T1 for read and write cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3, Tw and T4. The signal active LOW S7 is an input which the 8087 monitors during 8086/8088 controll of bus cycles.
$\overline{\text{S2}}$,$\overline{\text{S1}}$,$\overline{\text{S0}}$	28,27,26	I/O	Status: For 8087 drive bus cycles, these status lines are encoded as follows; S2 S1 $\overline{\text{S0}}$ 0(LOW) X X Unused 1(HIGH) 0 0 Unused 1 0 1 Read memory 1 1 0 Write memory 1 1 1 Passive Status is driven active during T4, remains valid during T1 and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 bus controller to generate all memory access control signals. Any change in S2, S1 or S0 during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals are monitored by the 8087 when the 8086/8088 is in control of the bus.

$\overline{\text{RQ}}/\overline{\text{GT0}}$	31	I/O	Request/Grant: This request/grant pin is used by the NDP to gain control of the local bus from the CPU for operand transfers or on behalf of another bus master. It must be connected to one of the two processor request/grant pins. The request grant sequence on this pin is as follows: 1.A pulse (one clock wide) is passed to the CPU to indicate a local bus request by either the 8087 or the master connected to the 8087 $\overline{\text{RQ}}/\overline{\text{GT1}}$ pin. 2.The NDP waits for the grant pulse. When it is received, it will either initiate bus transfer activity in the clock cycle following the grant or pass the grant out on the $\overline{\text{RQ}}/\overline{\text{GT1}}$ pin in this clock. In this case the initial request was for another bus master. 3.The 8087 will generate a release pulse to the CPU one clock after the completion of the last NDP bus cycle or on receipt of the release pulse from the bus master on $\overline{\text{RQ}}/\overline{\text{GT1}}$.
$\overline{\text{RQ}}/\overline{\text{GT1}}$	33	I/O	Request/Grant: This request/grant pin is used by another local bus master to force the NDP to release the local bus as the end of the processor's current bus cycle. If the NDP is not in control of the bus when the request is made, the request/grant sequence is passed through the NDP on the RQ/GT0 pin one cycle later. Subsequent grant and release pulses are also passed through the NDP with a two and one clock delay respectively, for resynchronization $\overline{\text{RQ}}/\overline{\text{GT1}}$ has an internal pull-up register, and so may be left unconnected. If the NDP has control of the bus, the request/grant sequence is as follows: 1.A pulse (1 CLK wide) from another local bus master indicates a local bus request to the 8077 (pulse 1) 2.During the NDP's next T4 or T1, a pulse (1 CLK wide) from the 8087 to the requesting master (pulse 2) indicates that the 8087 has allowed the local bus to float and that it will enter the "RQ/GT acknowledge" state at the next CLK. The NDP's control unit is disconnected logically from the local bus during "RQ/GT acknowledge."

			3.A pulse (1 CLK wide) from the requesting master indicates to the 8087 (Pulse 3) that the "RQ/GT" request is about to end and that the 8087 can reclaim the local bus as the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.
QS1,QSO	24,25	I	QS1,QSO: QS1 and QSO provide the 8087 with status to allow tracking of the CPU instruction queue. QS1 QSO 0(LOW) 0 No operation 0 1 First byte of op code from queue 1(HIGH) 0 Empty the queue 1 1 Subsequent byte from queue
INT	32	0	Interrupt: This line is used to indicate that an unmasked exception has occurred during numeric instruction execution when 8087 interrupts are enabled. This signal is typically routed to an 8259A. INT is active HIGH.
BUSY	23	0	Busy: This signal indicates that the 8087 NEU is executing a numeric instruction. It is connected to the CPU's TEST pin to provide CPU-NDP synchronization. In the case of an unmasked exception BUSY remains active until the exception is cleared. BUSY is active HIGH.
READY	22	I	Ready: READY is the acknowledgment from the address memory device that it will complete the data transfer. The RDY signal from memory is synchronized by the GAMYMC clock generator to/from READY. This signal is active HIGH.
RESET	21	I	Reset: RESET causes the processor to immediately terminate present activity. The signal must be active HIGH for at least four clock cycles. RESET is interally synchronized.
CLK	19	I	Clock: The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.

MB89322B

Figure 7-23 shows the MB89322B pin diagram, and Table 7-27 lists the pin descriptions for this IC. 〈B

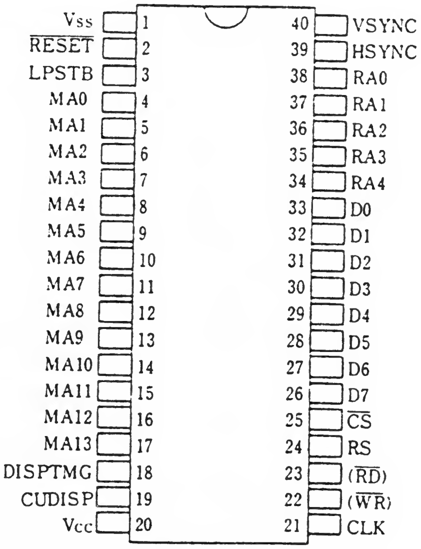

FIGURE 7-23. MB89322B PIN DIAGRAM

TABLE 7-27. MB89322B PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	Vss	-	Ground.
2	$\overline{\text{RES}}$	IN	Reset signal input.
3	LPSTB	IN	Light pen strobe signal input. Not used in the EQUITY II.
4-17	MA0-MA13	OUT	VRAM memory address signals.
18	DISPTMG	OUT	Active high timing signal used to define active display area.
19	CUDISP	OUT	Active high cursor timing signal.
20	Vcc	-	+5V supply connection.
21	CLK	IN	Timing clock. 1MHz: 40 column display 2MHz: 80 column display
22	R/W	IN	Read/write signal.
23	E	IN	Enable signal for read/write operations.
24	RS	IN	Register select signal.
25	$\overline{\text{CS}}$	IN	Active low chip select signal.
26-33	D0-7	IN/OUT	Bidirectional data bus signals.
34-38	RA0-RA4	OUT	Row address signals for gate arrays character generator to select correct scan row.
39	HSYNC	OUT	Horizontal sync output.
40	VSYNC	OUT	Vertical sync output.

LIST OF DIAGRAMS

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A-9	MCY-MT MOTHER BOARD
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A-11	SD-521 MAIN CONTROL BOARD CIRCUIT DIAGRAM
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A-14	SD-581L MAIN CONTROL BOARD CIRCUIT DIAGRAM
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A-17	KEYBOARD
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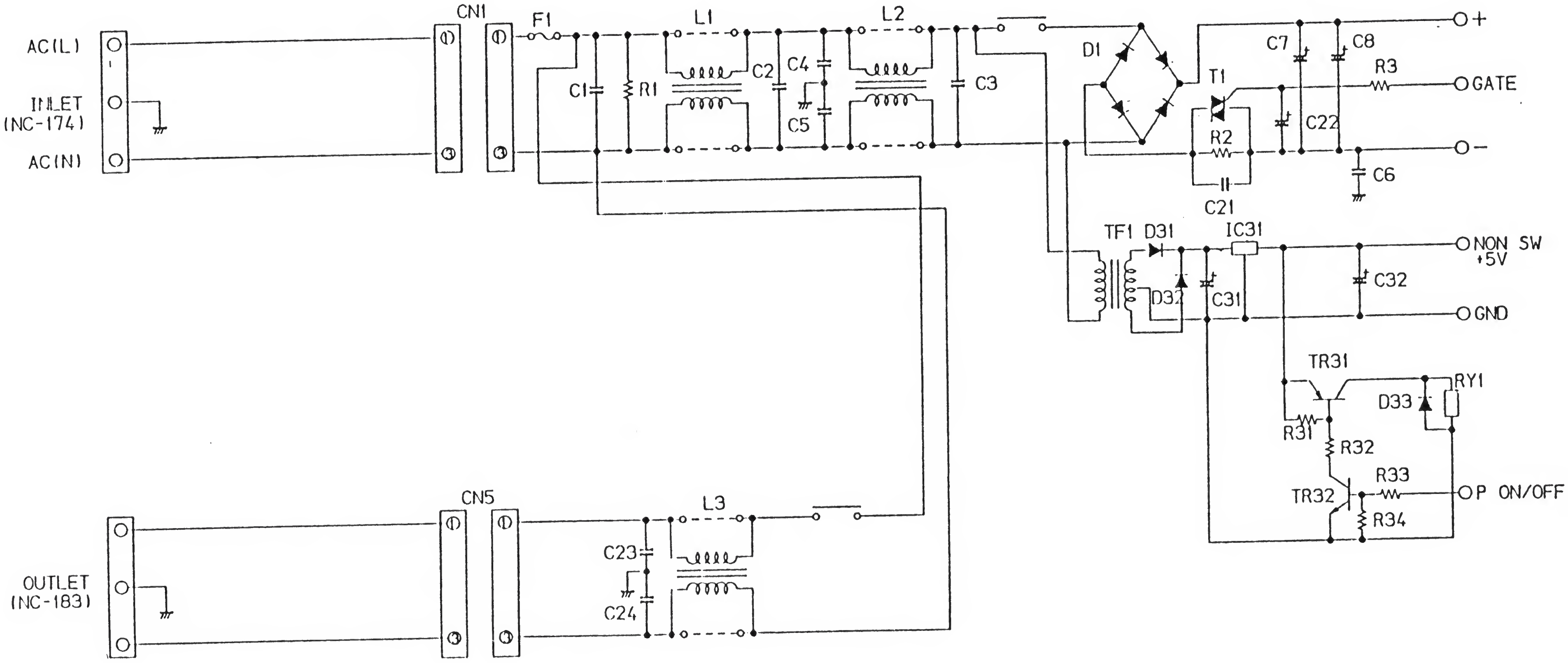
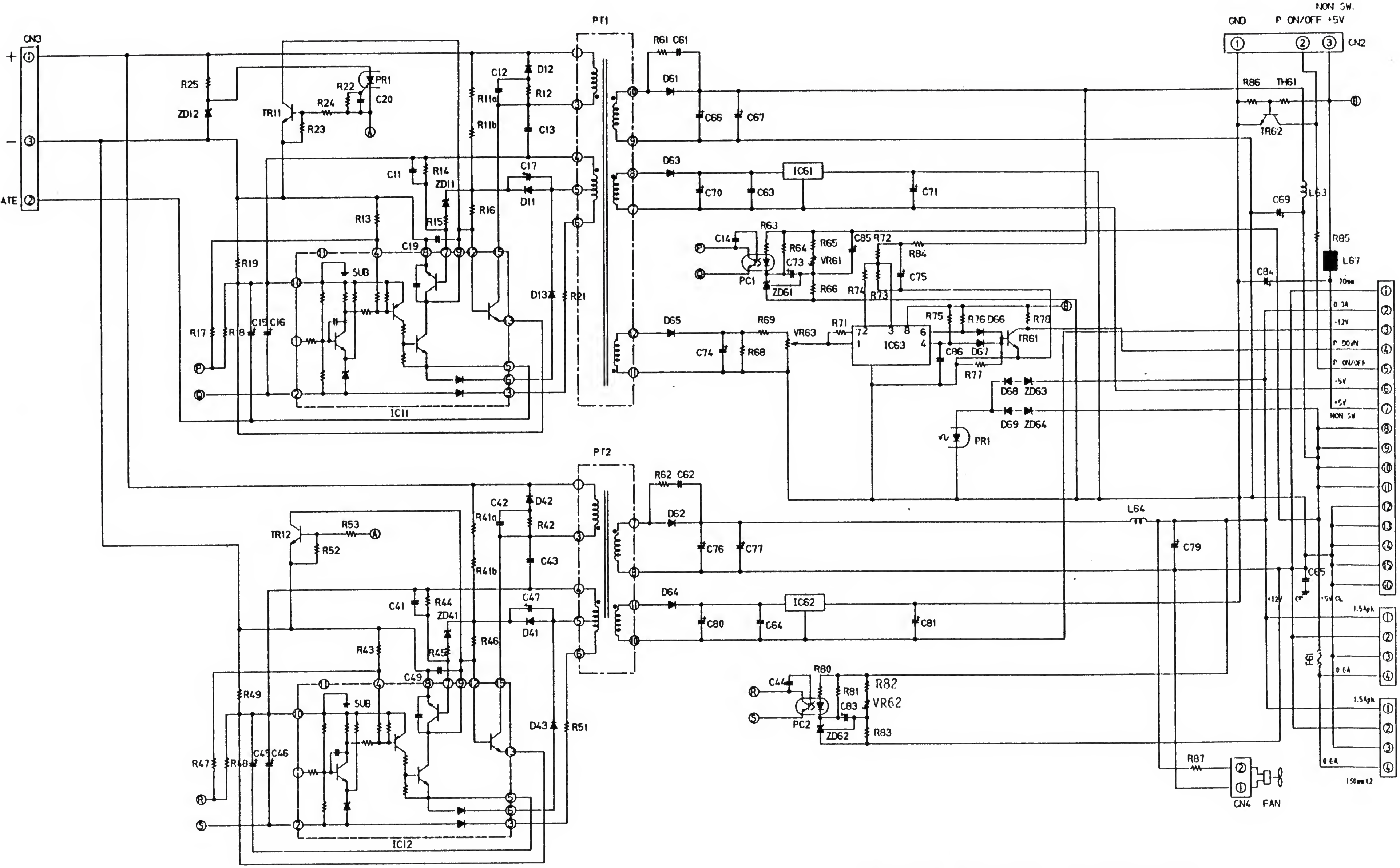
A-19	MCY MAIN CONTROL BOARD (SHEET 2/4)
A-20	MCY MAIN CONTROL BOARD (SHEET 3/4)
A-21	MCY MAIN CONTROL BOARD (SHEET 4/4)



MCYPSE UNIT
MCYPSE-AC-A BOARD



MCYPSE UNIT

MCYPS-DC-E BOARD

PARTS LIST MCYPSE

REF	NAME OF PARTS	SPECIFICATION	MAKER
	A. AC-LINE WIRING PARTS		
	Inlet	NC-174 UL E69198 CSA LR43108	NICOON
	Outlet	NC-183 UL E38319 CSA LR43108	NICOON
	Wire	UL1015, CSA TEW AWG ≠18 UL1015, CSA TEW AWG ≠18	FUJIKURA DAIWA
	Connector	5265-03, 5127-03 UL E29179 CSA LR37272	MOLEX
	B. INPUT PCB PARTS		
	PCB	MCYPSE-AC-A UL E48974A	SHINWA PRINT
	Jumping Wire	Copper wire 0.6 ϕ	
	B-1. Primary Parts		
F1	Fuse	SET. 3.15A 250V	S.O.C
	Fuse Holder	85PN0819	FMP
CN1	Connector	5285-03A UL E29179 CSA LR37272	MOLEX
CN5	Connector	5277-03A UL E29179 CSA LR37272	MOLEX
L1	Line filter	LF-5	TOP
L2	Jumping Wire		
L3	Line filter	LF-5	TOP
D1	Bridge Rectifier	DBA 40 G	SANYO
T1	Bidirectional Thyristor	DTA10E or G	SANYO
C1	Metallized Film Capacitor	ECQ-EW, 0.22 μF UL E62674 CSA LR35752	MATSUSHITA
C2	N.C		
C3	N.C		
C4	Ceramic Capacitor	DE7100F222MVA1-KC UL E37921	MURATA
C5	Ceramic Capacitor	DE7100F222MVA1-KC LR36214	MURATA
C6	Ceramic Capacitor	DE7100F222MVA1-KC	MURATA
C23	Ceramic Capacitor	DE7090B102KVA1-KC	MURATA
C24	Ceramic Capacitor	DE7090B10.2. VA1-KC	MURATA
C7	Electrolytic Capacitor	150 μF/400V	NIPPON CEMI-CON
C8	Electrolytic Capacitor	150 μF/400V	NIPPON CEMI-CON

REF	NAME OF PARTS	SPECIFICATION	MAKER
	B-1. Primary Parts		
C21	Film Capacitor	0.22 μF/400 V	RUBYCON
C22	Electrolytic Capacitor	470 μF/10V	
R1	Carbon Film Resistor	1MΩ, 1/2W	AKAHANE
R2	Temp.Fuse Resistor	22 Ω/5W	UMIKO
R3	Carbon Film Resistor		
	Connector	5265-03	MOLEX
		UL E29179	
		CSA LR37272	
	Wire	UL1015, CSA TEW AWG ♯18	FUJIKURA
		UL1015, CSA TEW AWG ♯18	DAIWA
	SIN Connector	SIN-21T-1.8	JST
	B-2. Between Primary and Secondary Parts		
TF1	Trans	TFY-MCYPS	KAMI Elec
RY1	Relay	G2R-2212P-FD-V-US	OMRON
		UL E41643	
		CSA LR31928	
	B-3. Secondary Parts		
IC31	3 Terminal Regulator	L78M05	SANYO
C31	Electrolytic Capacitor	470 μF/35V	MARCON
C32	Electrolytic Capacitor	4700 μF/10V	MARCON
R31	Carbon Film Resistor	1KΩ, 1/4W	AKAHANE
R32	Carbon Film Resistor	1KΩ, 1/4W	AKAHANE
R33	Carbon Film Resistor	5.1KΩ, 1/4W	AKAHANE
R34	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
TR31	Transistor	2SB544	SANYO
TR32	Transistor	2SC1570	SANYO
D31	Diode	DFC10E or G	SANYO
D32	Diode	DFC10E or G	SANYO
D33	Diode	DFD05C, E or G	SANYO
	Connector	5127-03	MOLEX
		UL E29179	
		CSA LR37272	
	Wire	UL1007, CSA TR-64 AWG ♯20	FUJIKURA
		UL1007, CSA TR-64 AWG ♯20	KAWASAKI
	SIN Connector	SIN-01T-1.8	
	Silicone-rubber sheet	TC-30A	SHIN-ETSU CHEMICAL
		UL E48923	
	Silicone-rubber compound	KE40RTV	
		UL E48923	

REF	NAME OF PARTS	SPECIFICATION	MAKER
C. POWER CONVERTER PCB PARTS			
	PCB	MCYPS-DC-E	CMK
	Jumping Wire	Copper Wire 0.6 φ	
	Jumping Wire	UL1430, CSA REW (XLPVC) AWG = 22	SUMITOMO Elec.
	IRRAX TUBE V2	Cat.No.806 UL E48762 CSA LR33298	SUMITOMO Elec.
	Silicone-rubber compound	KE40RTV UL E48923	
	C-1. Primary Parts		
IC11	Power Switch IC	STK7358	SANYO
IC12	Power Switch IC	STK7358	SANYO
D11	Diode	DFD05C, E or G	SANYO
D12	Diode	DFC10 G	SANYO
D13	Diode	DFD05C, E or G	SANYO
D41	Diode	DFD05C, E or G	SANYO
D42	Diode	DFC10 G	SANYO
D43	Diode	DFD05C, E or G	SANYO
ZD11	Zener Diode	GZA9.1Y	SANYO
ZD12	Zener Diode	GZA11Y	SANYO
ZD41	Zener Diode	GZA7.5 Y	SANYO
TR11	Transistor	2SC3070	SANYO
TR12	Transistor	2SC3070	SANYO
C11	Film Capacitor	0.1 μF/50V (0.01 μF to 0.22 μF ADJ)	Rubycon
C12	Ceramic Capacitor	0.01 μF/1KV	MURATA
C13	Ceramic Capacitor	DE7100F222MVA1-KC	MURATA
C14	Ceramic Capacitor	47PF/50V (1 to 1000pF/50V ADJ)	MURATA
C15	Electrolytic Capacitor	47 μF/16V	MARCON
C16	Electrolytic Capacitor	22 μF/50V	MARCON
C17	Electrolytic Capacitor	2.2μF/50V	MARCON
C19	N.C		
C20	Ceramic Capacitor	0.01 μF/50V	MURATA
C41	Film Capacitor	0.056 μF/50V (0.01 μF to 0.22 μF ADJ)	Rubycon
C42	Ceramic Capacitor	0.01 μF/1KV	MURATA
C43	Ceramic Capacitor	DE7100F222MVA1-KC	MURATA
C44	Ceramic Capacitor	470PF/50V (1 to 1000PF ADJ)	MURATA
C45	Electrolytic Capacitor	47 μF/16V	MARCON
C46	Electrolytic Capacitor	22 μF/50V	MARCON
C47	Electrolytic Capacitor	0.47 μ/50V (0.1 μF to 10 μF ADJ)	MARCON
C49	N.C		
R11a	Metal Film Oxide Resistor	100KΩ 1W	MATSUSHITA
R11b	Metal Film Oxidf Resistor	100KΩ 1W	MATSUSHITA
R12	Metal Film Oxidf Resistor	22KΩ 2W	MATSUSHITA
R13	Carbon Film Resistor	~~1K~~ Ω (100Ω to 10KΩ ADJ) 820 1/4W	AKAHANE

REF	NAME OF PARTS	SPECIFICATION	MAKER
	C-1. Primary Parts		
R14	Carbon Film Resistor	3.3K Ω, 1/4W	AKAHANE
R15	Carbon Film Resistor	240Ω (100Ω to 1K Ω ADJ) 1/4W	AKAHANE
R16	Metal Film Oxide Resistor	100Ω, 1W	MATSUSHITA
R17	Carbon Film Resistor	8.2K Ω (1K Ω to 10K Ω ADJ) 1/4W	AKAHANE
R18	Carbon Film Resistor	4.3K Ω (1K Ω to 10K Ω ADJ) 1/4W	AKAHANE
R19	Wound Resistor	0.47 Ω, 3W	JRM
R21	Fuse Resistor	10 Ω, 1/4W	HOKURIKU
R22	Carbon Film Resistor	12KΩ (1K Ω to 100K Ω ADJ) 1/4W	AKAHANE
R23	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R24	Carbon Film Resistor	2K Ω, 1/4W	AKAHANE
R25	Metal Film Oxide Resistor	100KΩ, 2W	MATSUSHITA
R41a	Metal Film Oxide Resistor	100KΩ, 1W	MATSUSHITA
R41b	Metal Film Oxide Resistor	100KΩ, 1W	MATSUSHITA
R42	Metal Film Oxide Resistor	22KΩ, 2W	MATSUSHITA
R43	Carbon Film Resistor	750Ω (100Ω to 10KΩ ADJ) 1/4W	AKAHANE
R44	Carbon Film Resistor	3.3K Ω, 1/4W	AKAHANE
R45	Carbon Film Resistor	270Ω (100Ω to 1K Ω ADJ) 1/4W	AKAHANE
R46	Metal Film Oxide Resistor	68 Ω, 2W	MATSUSHITA
R47	Carbon Film Resistor	3.2K Ω (1K Ω to 10K Ω ADJ) 1/4W	AKAHANE
R48	Carbon Film Resistor	4.7K Ω (1K Ω to 10K Ω ADJ) 1/4W	AKAHANE
R49	Wound Resistor	0.47 Ω, 3W	JRM
R51	Fuse Resistor	10 Ω, 1/4W	HOKURIKU
R52	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R53	Carbon Film Resistor	1.2K Ω, 1/4W	AKAHANE
CN3	Connector	5277-03A UL E29179 CSA LR37272	MOLEX
	Silicone-rubber sheet	TC-80A UL E48923	SHIN-ETSU CHEMICAL
	C-2. Between Primary and Secondary Parts		
PT1	Pulse Transformer	PTY-MCY-A	TOP
PT2	Pulse Transformer	PTY-MCY-B	TOP
PC1	Photo Coupler	PC713	SHARP
PC2	Photo Coupler	PC713 }UL E64380	SHARP
PR1	Photo Relay	S22MD1	SHARP

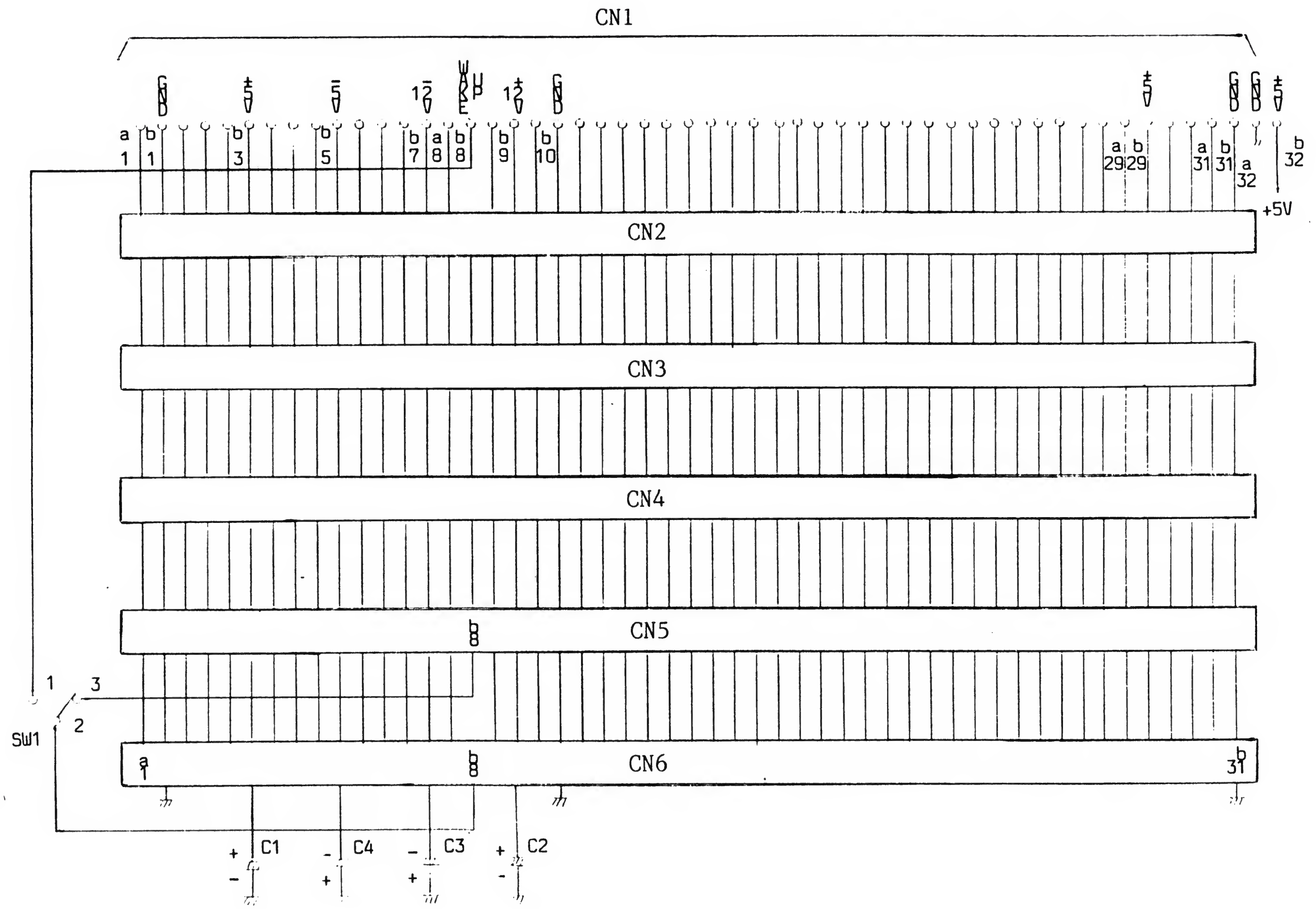
REF	NAME OF PRATS	SPECIFICATION	MAKER
	C-3. Secondary Parts		
D61	Diode	ESAC82-004	FUJI Elec.
D62	Diode	ESAB92-02	FUJI Elec.
D63	Diode	DFC10E or G	SANYO
D64	Diode	DFC10E or G	SANYO
D65	Diode	DS442	SANYO
D66	Diode	DS442	SANYO
D67	Diode	DS442	SANYO
D68	Diode	DS442	SANYO
D69	Diode	DS442	SANYO
ZD61	Shunt Regulator	TL431	TI
ZD62	Shunt Regulator	TL431	TI
ZD63	Zener Diode	GZA12Y	SANYO
ZD64	Zener Diode	GZA4.7X, Y or Z	SANYO
TR61	Transistor	2SC1570	SANYO
TR62	Transistor	2SC1570	SANYO
IC61	3 Terminal Regulator	L78M05	SANYO
IC62	3 Terminal Regulator	L78M12	SANYO
IC63	Comparater IC	MB3761	FUJITSU
L63 ,	Inductor	PI- 3	TOP
L64	Inductor	SN5.3 μH-0.8	TOKYO PARTS
L67	Ferrite bead	OP28 7-06124	TOP
C61	N.C		
C62	N.C		
C63	Ceramic Capacitor	0.01 μF/50V	MURATA
C64	Ceramic Capacitor	0.01 μF/50V	MURATA
C65	Ceramic Capacitor	0.01 μF/1KV	MURATA
C66	Electrolytic Capacitor	4700 μF/10V	MARCON
C67	Electrolytic Capacitor	4700 μF/10V	MARCON
C69	Electrolytic Capacitor	4700 μF/10V	MARCON
C70	Electrolytic Capacitor	470 μF/16V	MARCON
C71	Electrolytic Capacitor	470 μF/10V	MARCON
C73	Electrolytic Capacitor	10 μF/50V	MARCON
C74	Electrolytic Capacitor	2.2 μF/50V	MARCON
C75	Electrolytic Capacitor	10 μF/50V	MARCON
C76	Electrolytic Capacitor	2200 μF/25V	MARCON
C77	Electrolytic Capacitor	2200 μF/25V	MARCON
C79	Electrolytic Capacitor	1000 μF/25V	MARCON
C80	Electrolytic Capacitor	470 μF/35V	MARCON
C81	Electrolytic Capacitor	470 μF/25V	MARCON
C83	Electrolytic Capacitor	10 μF/50V	MARCON
C84	Electrolytic Capacitor	47 μF/25V	MARCON
C85	Electrolytic Capacitor	4.7 μF/50V (0.1 μF to 22 μF ADJ)	MARCON
C86	Film Capacitor	0.01 μF/50V	Rubycon
R61	N.C		
R62	N.C		
R63	Carbon Film Resistor	100Ω, 1/4W	AKAHANE
R64	Carbon Film Resistor	100Ω, 1/4W	AKAHANE
R65	Carbon Film Resistor	1K Ω, 1/4W	AKAHANE
R66	Carbon Film Resistor	1.5K Ω, 1/4W	AKAHANE
R68	Carbon Film Resistor	1K Ω, 1/4W	AKAHANE
R69	Carbon Film Resistor	20K Ω, 1/4W	AKAHANE

REF	NAME OF PARTS	SPECIFICATION	MAKER
	C-3. Secondary Parts		
R71	Carbon Film Resistor	43KΩ, 1/4W	AKAHANE
R72	Carbon Film Resistor	47KΩ, 1/4W	AKAHANE
R73	Carbon Film Resistor	33KΩ, 1/4W	AKAHANE
R74	Carbon Film Resistor	330K Ω (10KΩ to 1M Ω ADJ) 1/4W	AKAHANE
R75	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R76	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R77	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R78	Carbon Film Resistor	5.1K Ω, 1/4W	AKAHANE
R80	Carbon Film Resistor	100Ω, 1/4W	AKAHANE
R81	Carbon Film Resistor	240Ω, 1/4W	AKAHANE
R82	Carbon Film Resistor	3.3K Ω, 1/4W	AKAHANE
R83	Carbon Film Resistor	1K Ω, 1/4W	AKAHANE
R84	Carbon Film Resistor	20KΩ (10KΩ to 33KΩ ADJ) 1/4W	AKAHANE
R85	Carbon Film Resistor	10KΩ, 1/4W	AKAHANE
R86	Carbon Film Resistor	110Ω, 1/4W	AKAHANE
R87	Jumping Wire		
VR61	Potentiometer	2K Ω	MURATA
VR62	Potentiometer	2K Ω	MURATA
VR63	Potentiometer	20K Ω	MURATA
F61	Fuse	SSFR4A UL E39255 CSA 34647	S.O.C
TH61	Thermistor	SDT500	SANYO
	Connector	PD 044-09M	OTP
CN2	Connector	5283-03A UL E29179	MOLEX
CN4	Connector	5045-02A CSA LR37272	MOLEX
	FAN	SJF-08Z12A	SEIZAIKEN
	Connector	5265-16	MOLEX
	Connector	MATE-N-LOK Series. 1-480424-0 UL E28476	AMP
	Wire	UL1007, CSA TR-64 AWG ≠20	FUJIKURA
		UL1007, CSA TR-64 AWG ≠20	KAWASAKI
	Silicone-rubber tube	TC-30A UL E48923	

NOTE

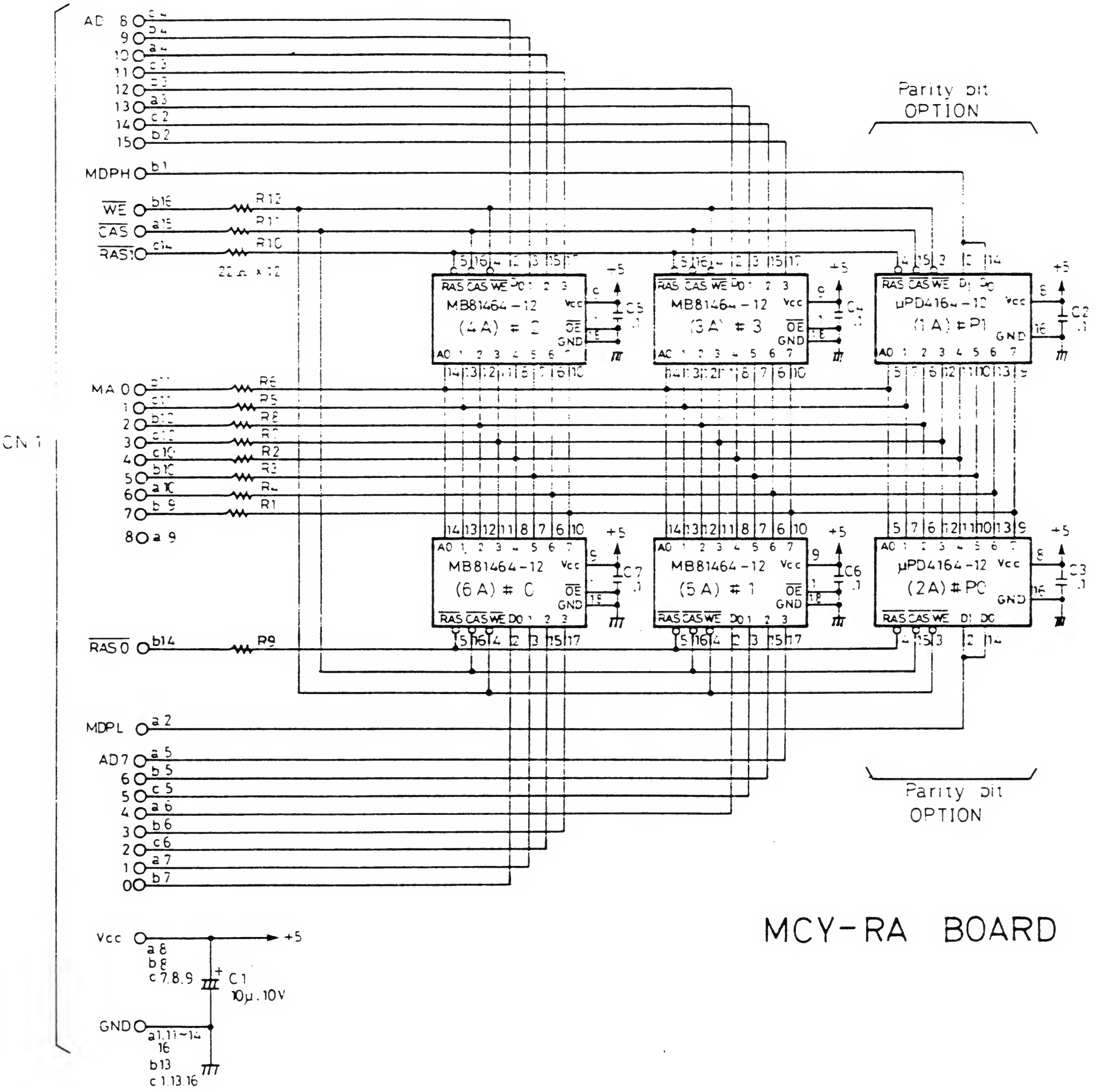
*** (*** to *** ADJ.)

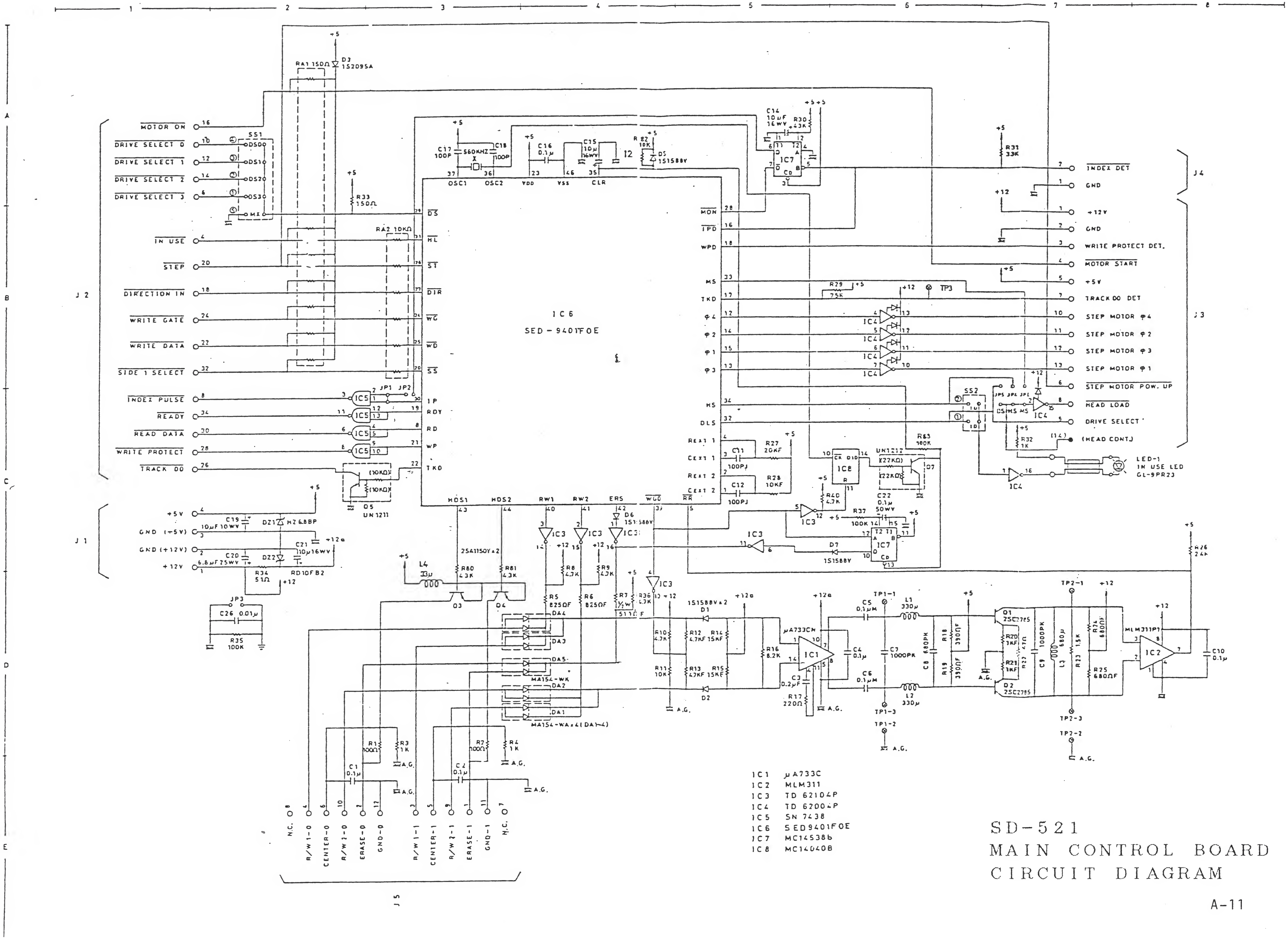
→ Typical value
→ Minimum value
→ Maximum value



MCY-MT MOTHER BOARD

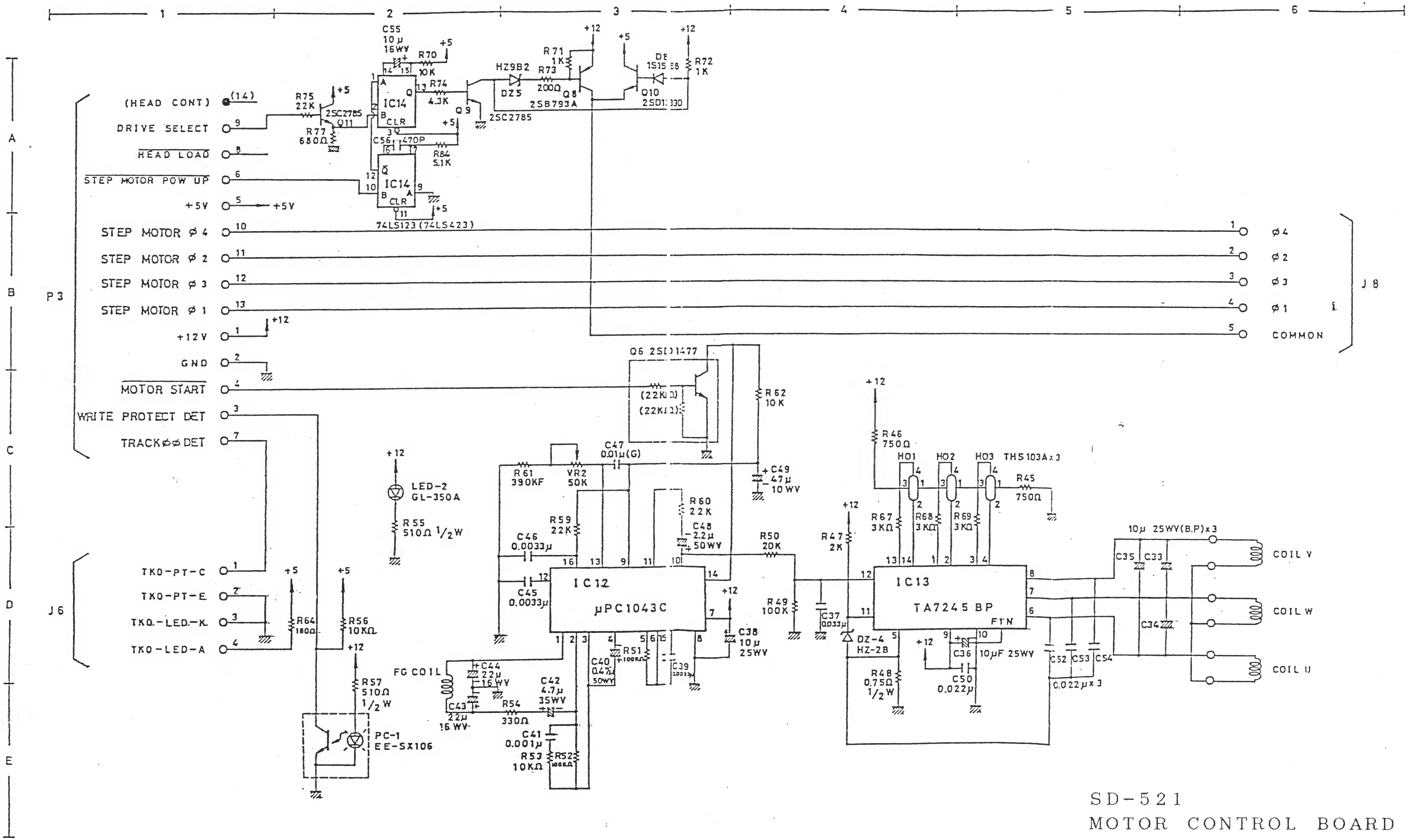
MAIN MEMORY UNIT (128KBYTE)



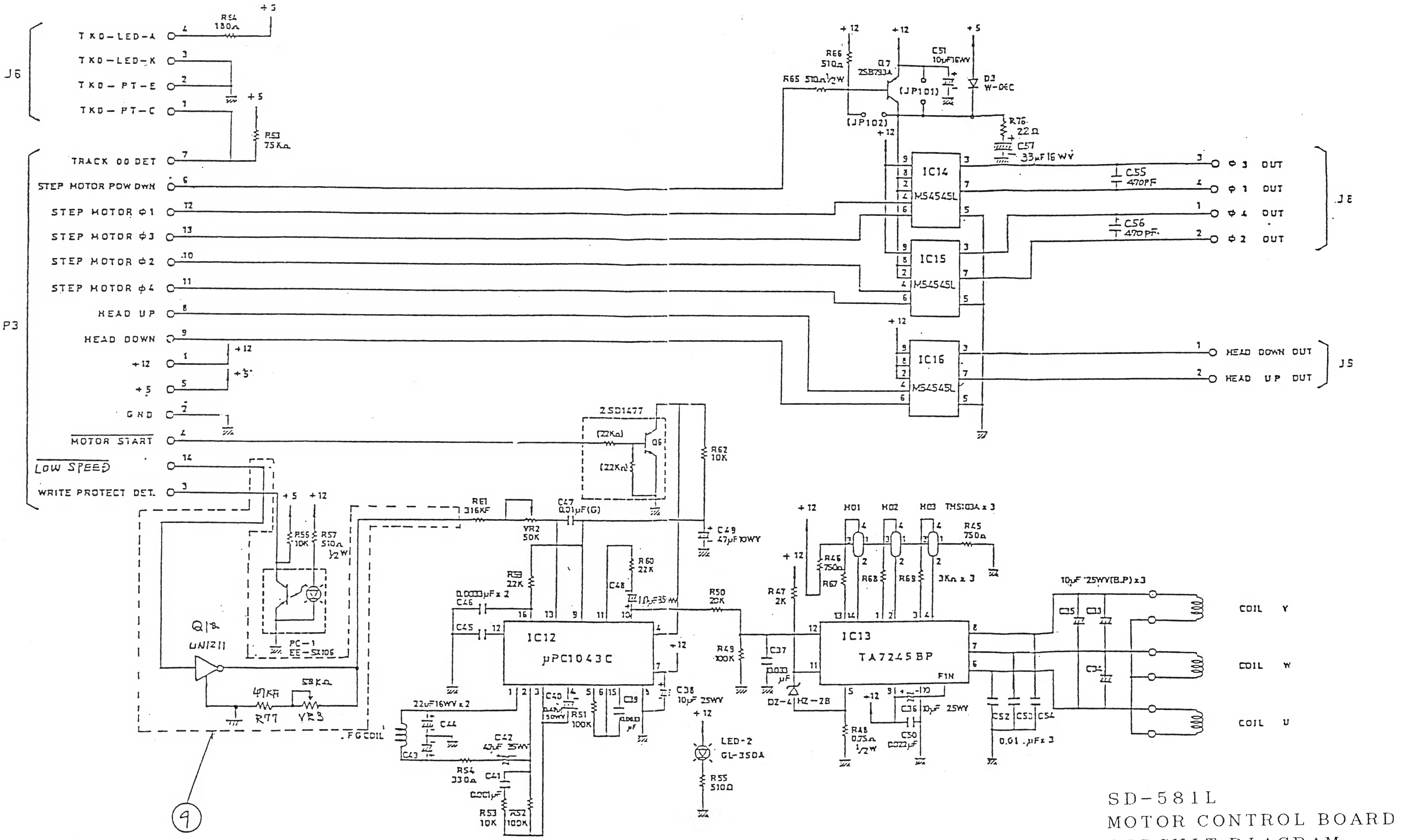


IC1	μA733C
IC2	MLM311
IC3	TD 62104P
IC4	TD 62004P
IC5	SN 7438
IC6	SED9401FOE
IC7	MC14538B
IC8	MC14040B

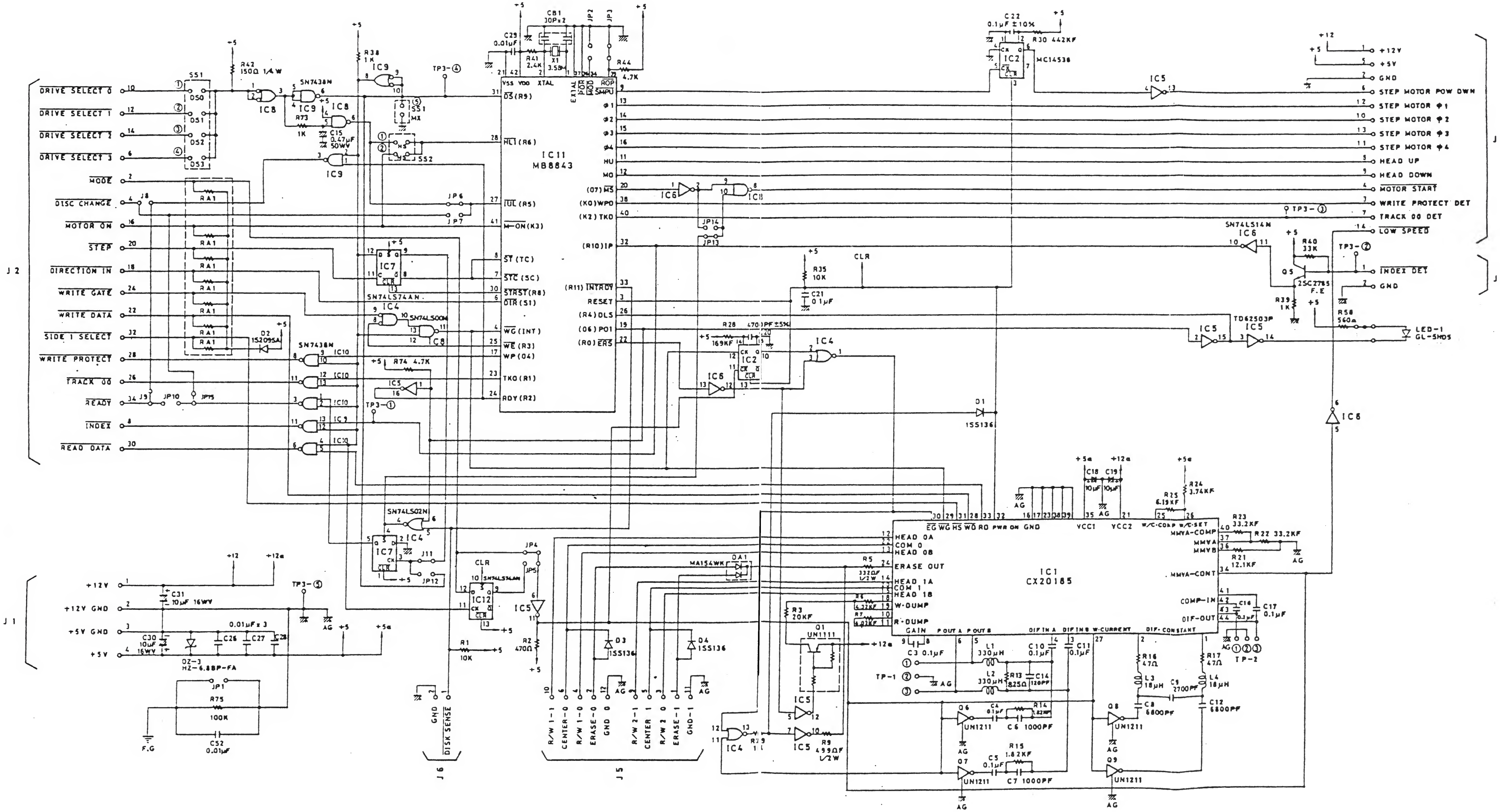
SD-521
MAIN CONTROL BOARD
CIRCUIT DIAGRAM



SD-521
MOTOR CONTROL BOARD
CIRCUIT DIAGRAM

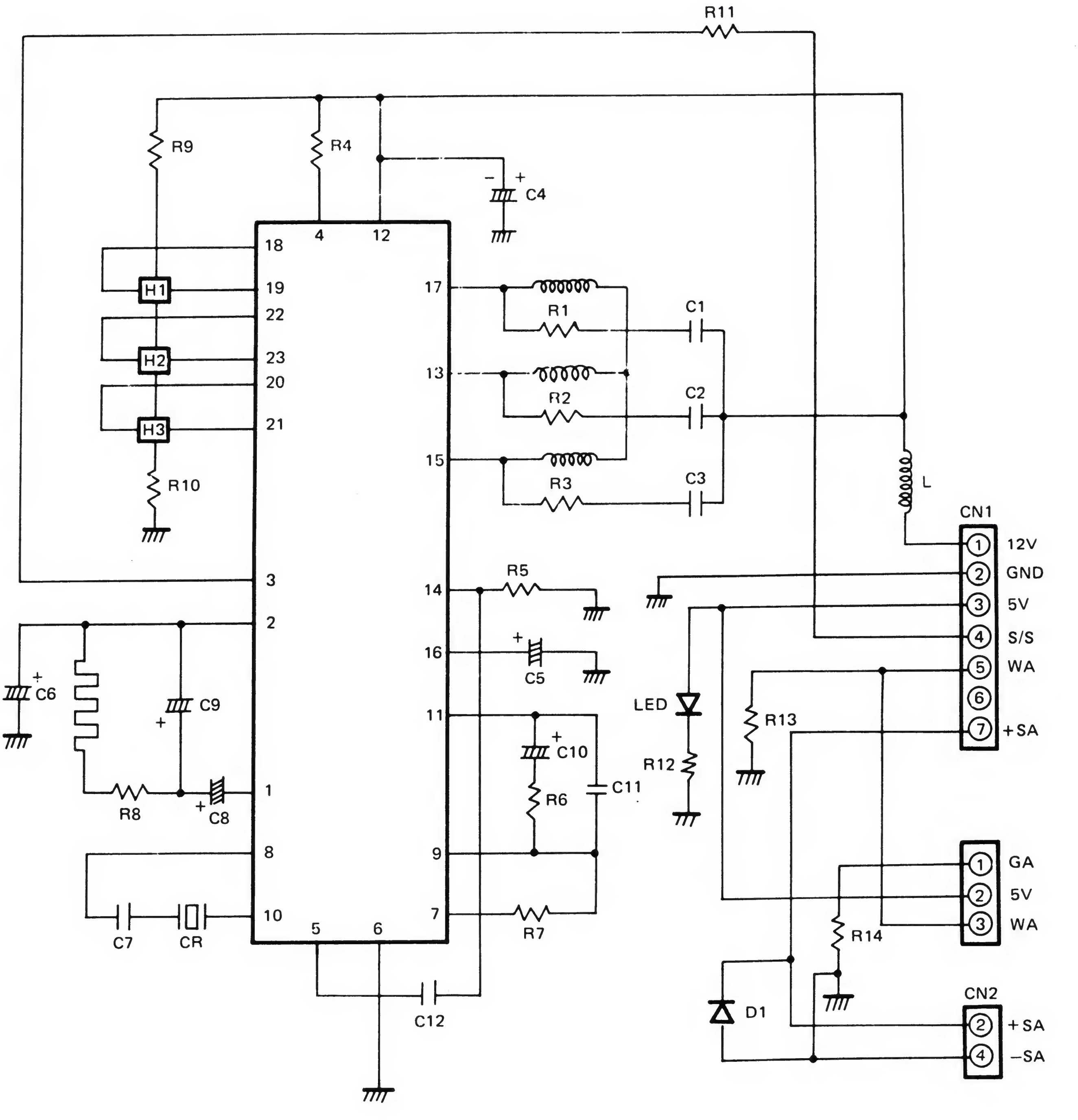


SD-581L
MOTOR CONTROL BOARD
CIRCUIT DIAGRAM

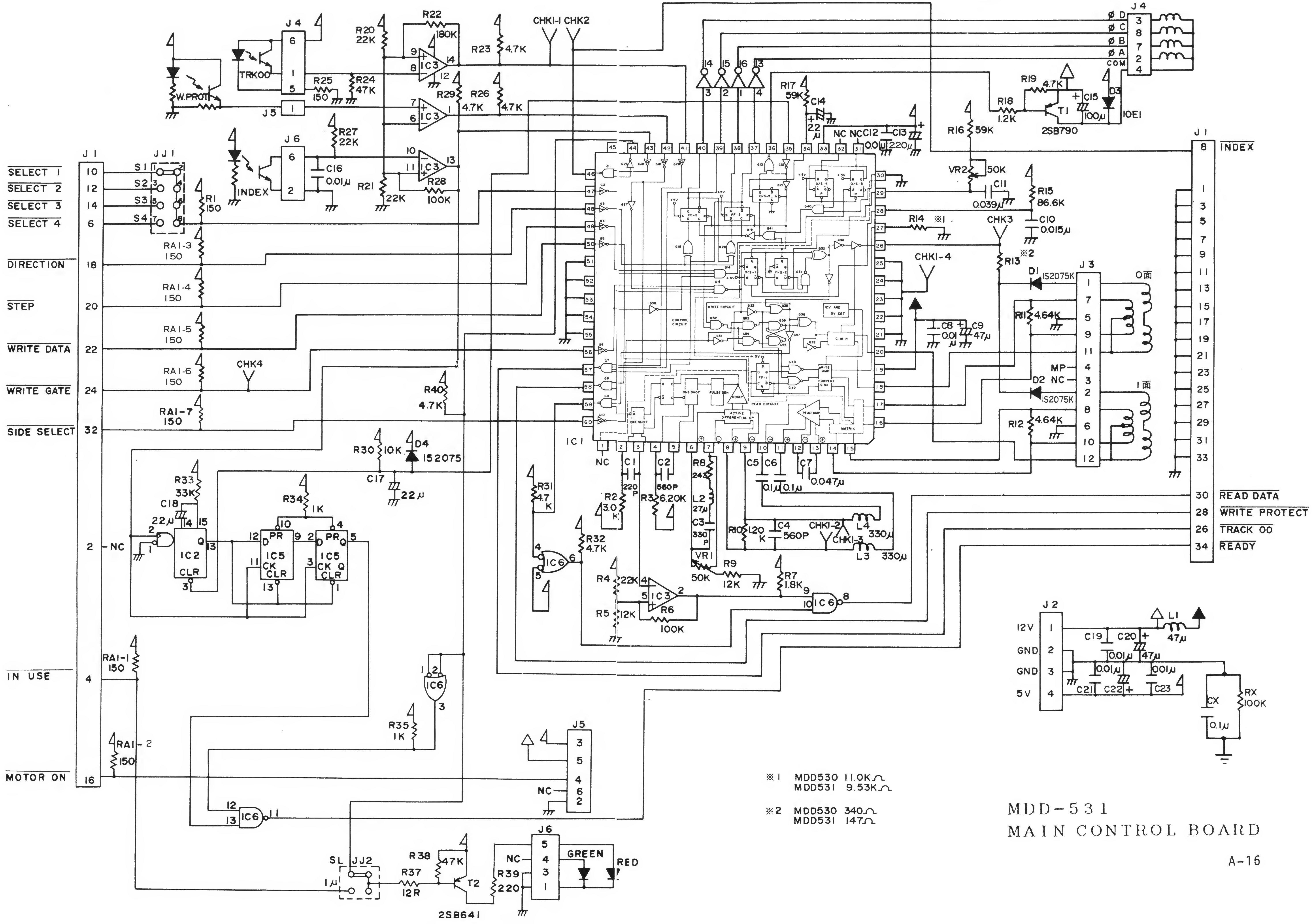


SD-581L
MAIN CONTROL BOARD
CIRCUIT DIAGRAM

A-14



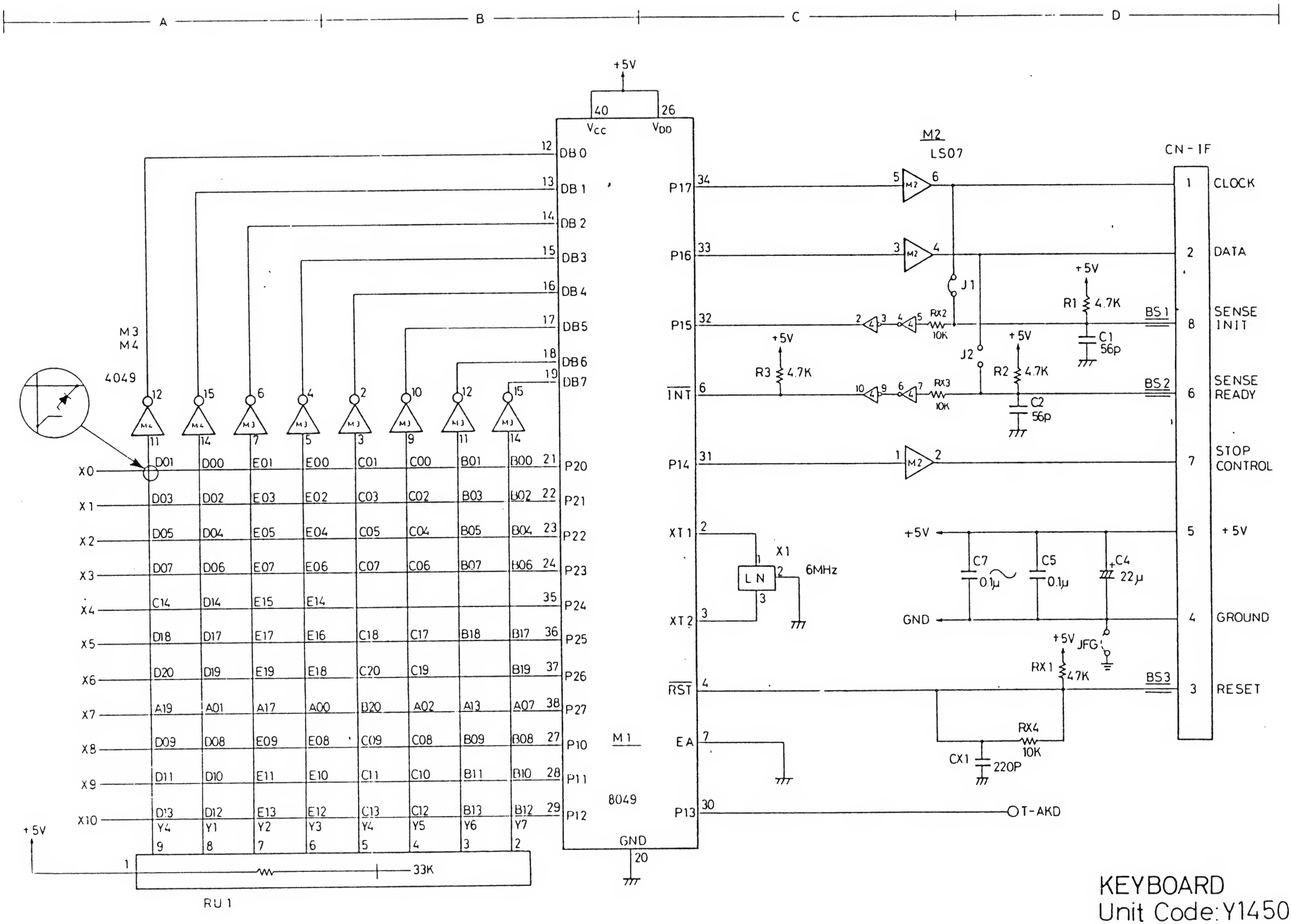
MDD−531
DD MOTOR
CIRCUIT DIAGRAM



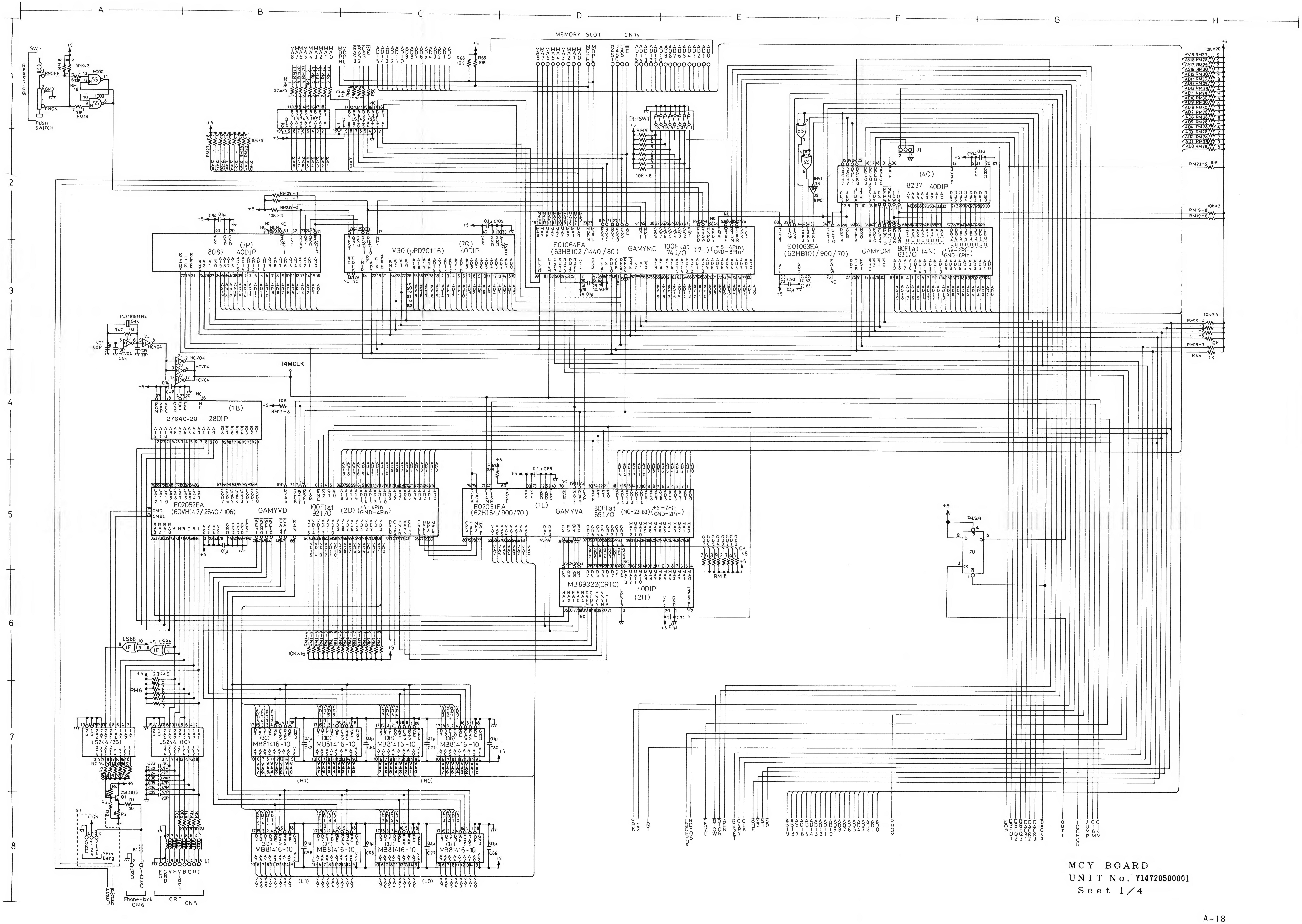
※1 MDD530 11.0KΩ
MDD531 9.53KΩ

※2 MDD530 340Ω
MDD531 147Ω

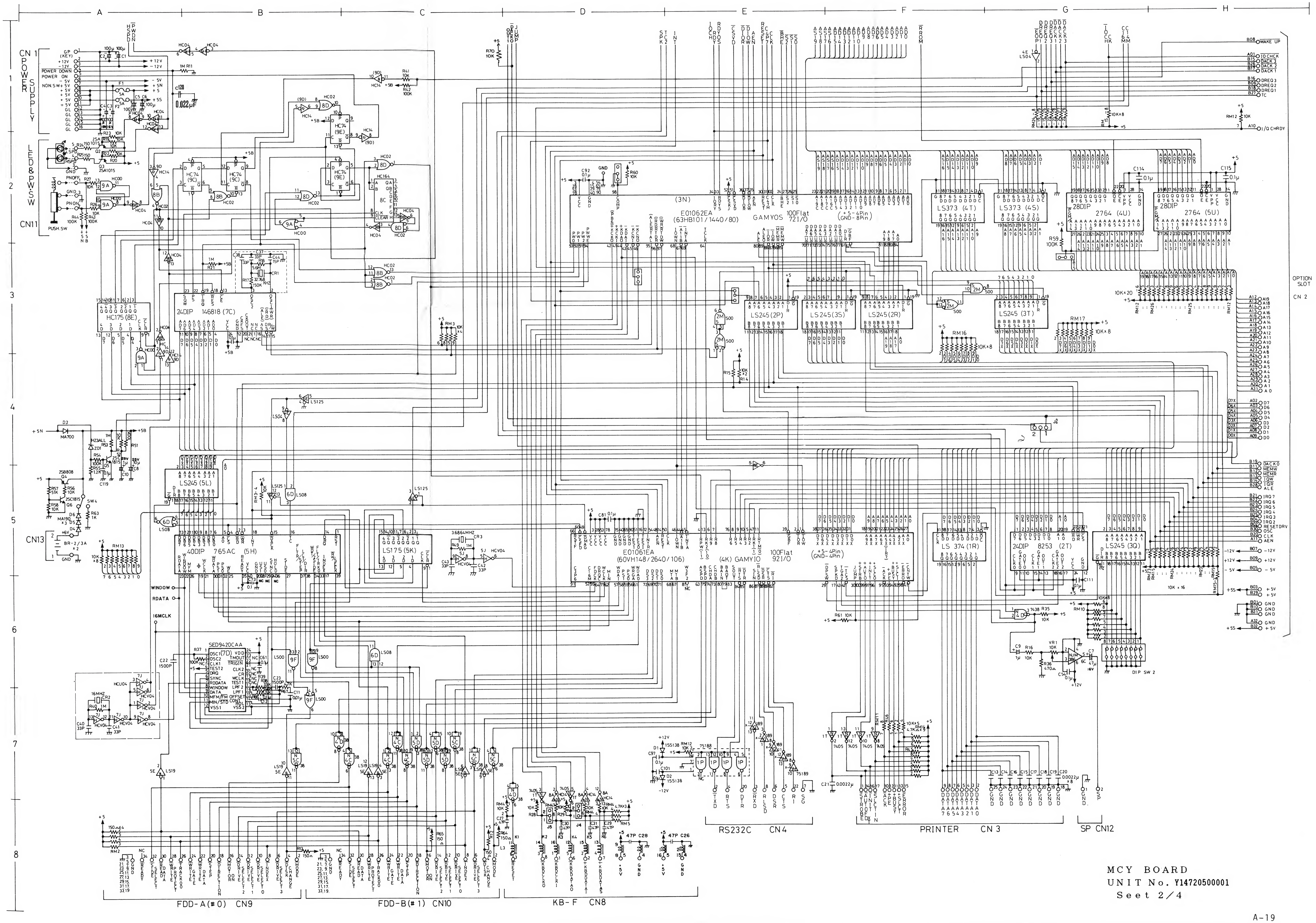
MDD-531
MAIN CONTROL BOARD



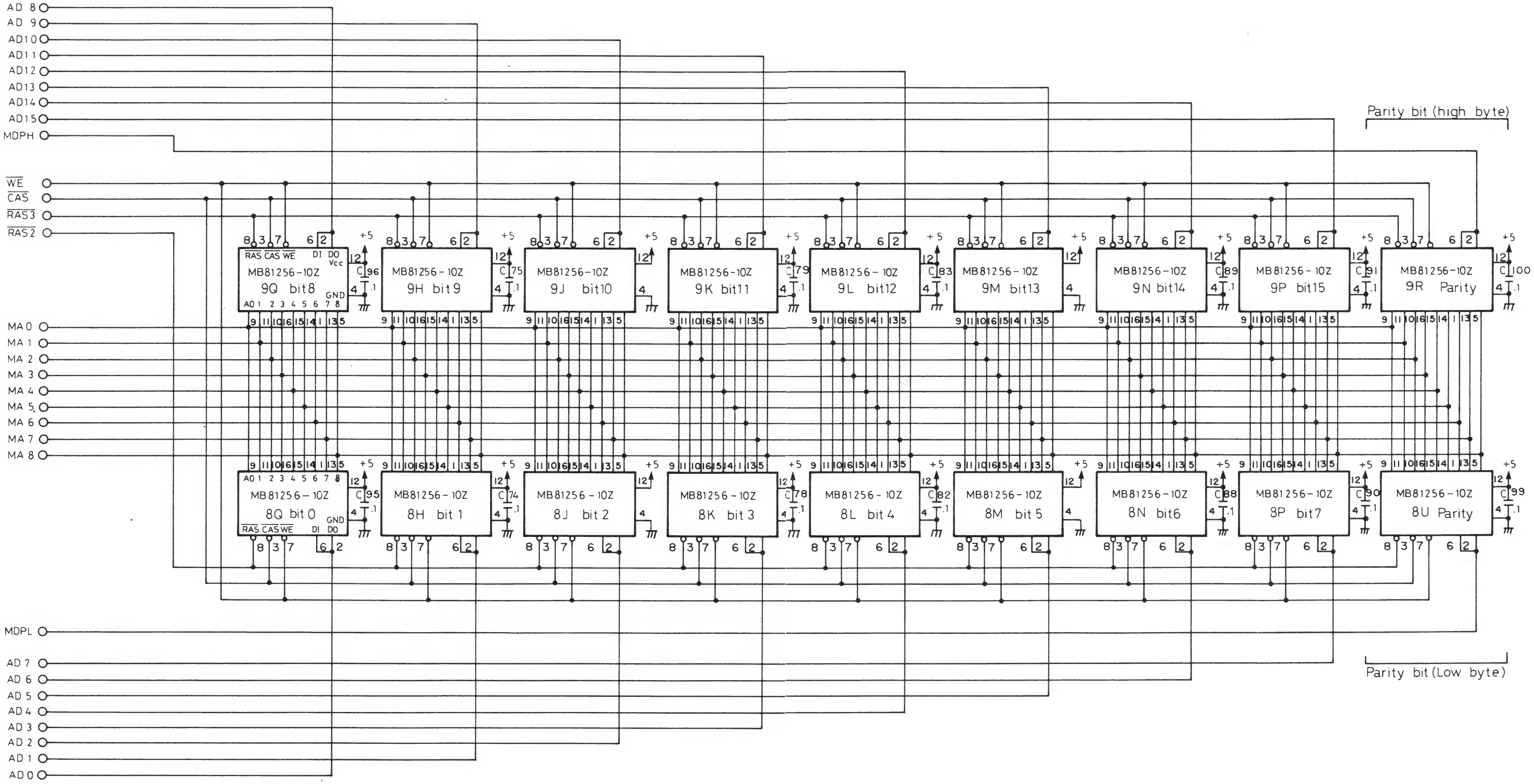
KEYBOARD
Unit Code: Y145010001



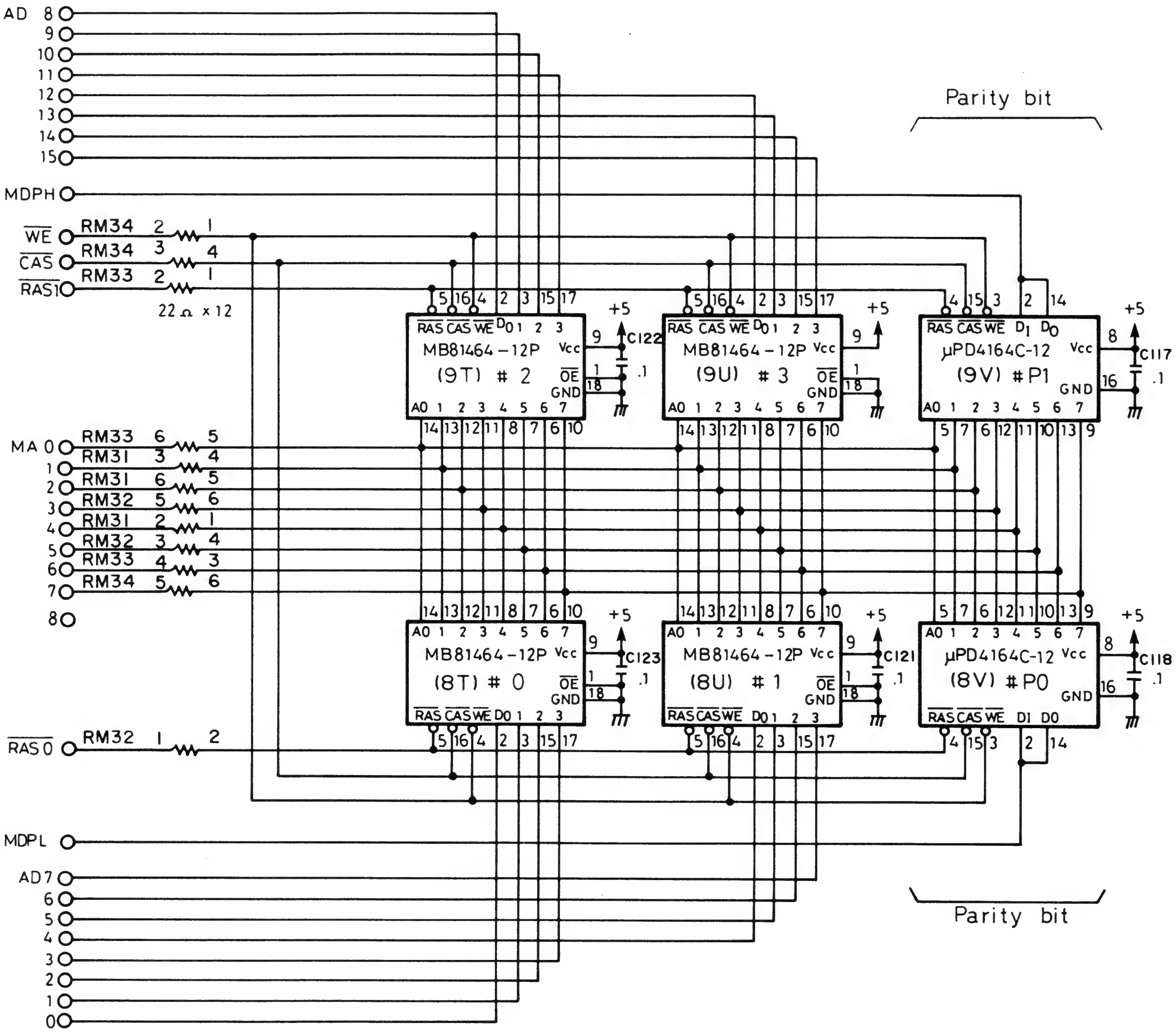
MCY BOARD
UNIT No. Y14720500001
Seet 1/4



MCY BOARD
UNIT No. Y14720500001
Seet 2/4



MCY BOARD
UNIT No. Y14720500001
Seet 3/4



MCY BOARD
UNIT No. Y14720500001
Seet 4/4

EPSON OVERSEAS MARKETING LOCATIONS

EPSON AMERICA, INC.
Building #6 23610 Telo Ave., Torrance
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Wembley, Middlesex, HA9 6UH, U.K.
Phone: 01-902-8892
Telex: 8814169

EPSON ITALY S.p.A.
Via Timavo, 12 20124 Milano
Phone: 02-6709136
Telex: 315132 SEGI I

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PARTS PRICE LIST

EPSON

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EQUITY II

PARTS PRICE LIST

November 24, 1987

(CONTENTS SUBJECT TO CHANGE WITHOUT NOTICE)

M-PL-EQII

SECTION: CASE COMPONENTS **MODEL:** EQUITY II

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
100	Y144012001	TOP COVER (144-1130)	1	80.50	
101	B010304512	C.B. SCREW (M4X8)	7	0.25	
102	Y144010001	SIDE STAND (144-1110)	2	3.50	
103	Y144011001	SCREW CAP (144-1120)	2	2.40	
104	Y147018001	OPTION BOARD HOLDER B (144-1310)	1	3.36	
105	Y144000201	BOTTOM COVER (144-1010)	1	33.60	
106	Y144001001	K.B. CONNECTOR LID (144-1020)	1	2.40	
107	Y147000001	BASE PLATE B (147-1050)	1	17.82	
108	Y144035001	DUMMY PLATE (144-1380)	1	1.40	
109	Y147001001	INSULATION B (147-1060)	1	8.96	
110	Y144002201	FRONT COVER C	1	14.94	
111	Y144004201	K.B. CONNECTOR COVER C	1	3.00	
112	Y144006201	POWER SWITCH COVER (144-1070)	1	5.12	
113	Y144005001	DIP SWITCH COVER (144-1060)	1	4.00	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
114	Y144025001	EARTH PLATE A (144-1300)	2	1.40	
115	Y144008001	REAR COVER (144-1090)	1	13.68	
116	Y147003001	REAR PLATE B (147-1080)	1	92.75	
117	B040450411	C.P.O. SCREW (M4X6)	5	0.25	
118	B043400211	CUP SCREW (S)(M3X6)	2	0.25	
119	B018102611	C.T.P. SCREW (M4X12)	4	0.25	
120	Y147001101	INSULATION C (147-1120)	1	3.60	
121	Y147001201	INSULATION D (147-1130)	1	3.50	
122	Y144014001	FRONT OPTION BOARD GUIDE (144-1150)	1	6.72	
123	B018201811	C.T.B. SCREW (M3X10)	20	0.25	
124	Y144018002	FDD FIXING PLATE (144-1190)	1	43.92	
125	Y126510000	LITHIUM BATTERY (2CL101)	1	52.55	
126	Y147002001	BATTERY FIXING PLATE (147-1052)	1	33.60	
127	Y137303000	CABLE SET 5AD	1	12.88	
128	Y911034001	CAUTION LABEL	1	0.40	

SECTION: CASE COMPONENTS **MODEL:** EQUITY II

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
129	Y901010101	UL-CSA LABEL	1	0.40	
130	Y147009001	P/S LABEL (147-1160)	1	0.70	FOR 120V
130	Y147009101	P/S LABEL (147-1160)	1	2.30	FOR 220/240V
131	Y147005001	SWITCH BUTTON (147-1100)	1	1.10	
132	Y144033001	INTERFACE LABEL (144-1360)	1	0.70	
133	Y147014001	INTERFACE LABEL 02 (147-1210)	1	0.70	
134	Y137013001	RESET BUTTON (137-1180)	1	1.10	
135	Y144508000	RUBBER STAND	4	0.60	
136	Y147202000	MCY-SW CIRCUIT BOARD UNIT	1	52.55	
137	Y147006001	OP. GUIDE PLATE B (147-1110)	1	2.80	
138	Y911005001	CODING LABEL AA	1	0.30	FOR 1FDD
138	Y911005101	CODING LABEL AB	1	0.30	FOR 1FDD.1HDD
139	Y144049001	EARTH PLATE FOR K.B CONNECTOR (144-1540)	1	2.10	
140	Y147015001	P.S. PANEL LABEL (147-1220)	1	3.50	FOR 120V
140	Y147015101	P.S. PANEL LABEL (147-1270)	1	2.30	FOR 220/240V

REF.NO.	**PART NO.**	**DESCRIPTION**	**QTY.**	**UNIT PRICE**	**REMARKS**
141	Y147010001	POWER SWITCH LABEL (147-1170)	1	1.10	
142	Y147012001	SWITCH PANEL LABEL (147-1190)	1	2.10	
143	Y147011001	DIP SWITCH SETTING LABEL B (147-1180)	1	2.80	
145	Y147013001	CONNECTOR PANEL B (147-1200)	1	2.80	
146	Y147007001	LOGO PLATE (147-1140)	1	1.80	"EQUITY II"
146	Y147007101	LOGO PLATE 02 (147-1140)	1	2.30	"EPSON PC+"
146	Y147007201	LOGO PLATE 03 (147-1140)	1	2.30	"EPSON PC+/HD"
147	Y144003001	DISK DRIVE COVER (144-1040)	1	4.24	FOR 1FDD
148	B018201811	C.T.B. SCREW (M3X10)	5	0.25	
149	Y144009001	OPTION BOARD COVER (144-1100)	5	2.40	
150	Y144020001	CONNECTOR GUIDE (144-1210)	5	2.80	
151	Y144038101	FIXING SCREW 2 (144-1460)	5	1.40	
152	B090600912	OUTSIDE TOOTHED LOCK WASHER (M4)	5	0.25	
153	Y144039001	FDD GUIDE SCREW (144-1420)	2	0.70	

REF.NO.	**PART NO.**	**DESCRIPTION**	**QTY.**	**UNIT PRICE**	**REMARKS**
154	Y144038001	FIXING SCREW (144-1410)	2	0.80	
155	B018101711	C.T.P. SCREW (M3X8)	1	0.25	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
200	Y147206000	MCY CIRCUIT BOARD UNIT	1	924.00	WITHOUT 4U, 5U
4U	Y147810802	P-ROM (ONE-TIME ROM MQA-B2)	1	53.90	
5U	Y147810702	P-ROM (ONE-TIME ROM MQA-A2)	1	53.90	
7Q	X400071160	LSI (8MHZ)	1	54.60	
1B	Y144300100	P-ROM (2764)	1	71.50	

SECTION: MCY-MT CONTROL CIRCUIT BOARD UNIT **MODEL:** EQUITY II

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
210	Y147203000	MCY-MT CIRCUIT BOARD UNIT	1	71.50	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
220	Y147204000	MCY-RA CIRCUIT BOARD UNIT	1	115.50	FOR U.S.A.

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
300	Y147501000	MCYPS UNIT	1	293.04	FOR 120V
301	Y901300600	POWER CABLE (100V/120V)	1	31.50	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
400	Q213A-AA	FDD MECH. (MD5201-57)	1	199.00	
401	Y147305000	CABLE SET #5BM	1	25.44	

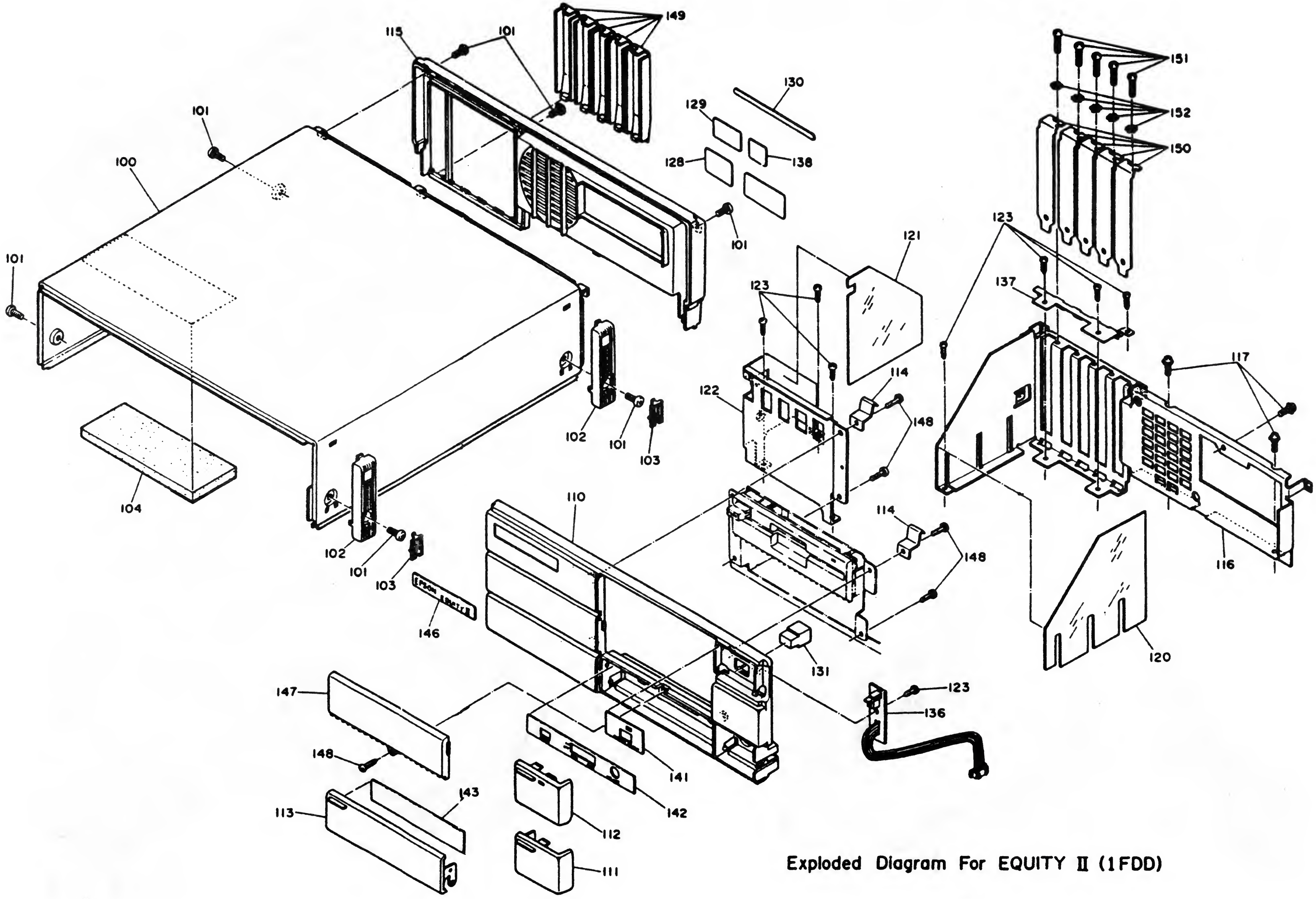
REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
501	Y144505001	HARD DISK CONTROLLER (WD1002S-WX2C027)	1	504.90	FOR 1FDD.1HDD
502	Y144308000	CABLE SET 5BC	1	26.10	FOR 1FDD.1HDD
503	Y144309000	CABLE SET 5BD	1	19.92	FOR 1FDD.1HDD
504	T800812000	FRONT PANEL UNIT (GRAY)	1	13.20	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
*	Y145501001	KEYBOARD CIRCUIT BOARD UNIT	1	161.70	

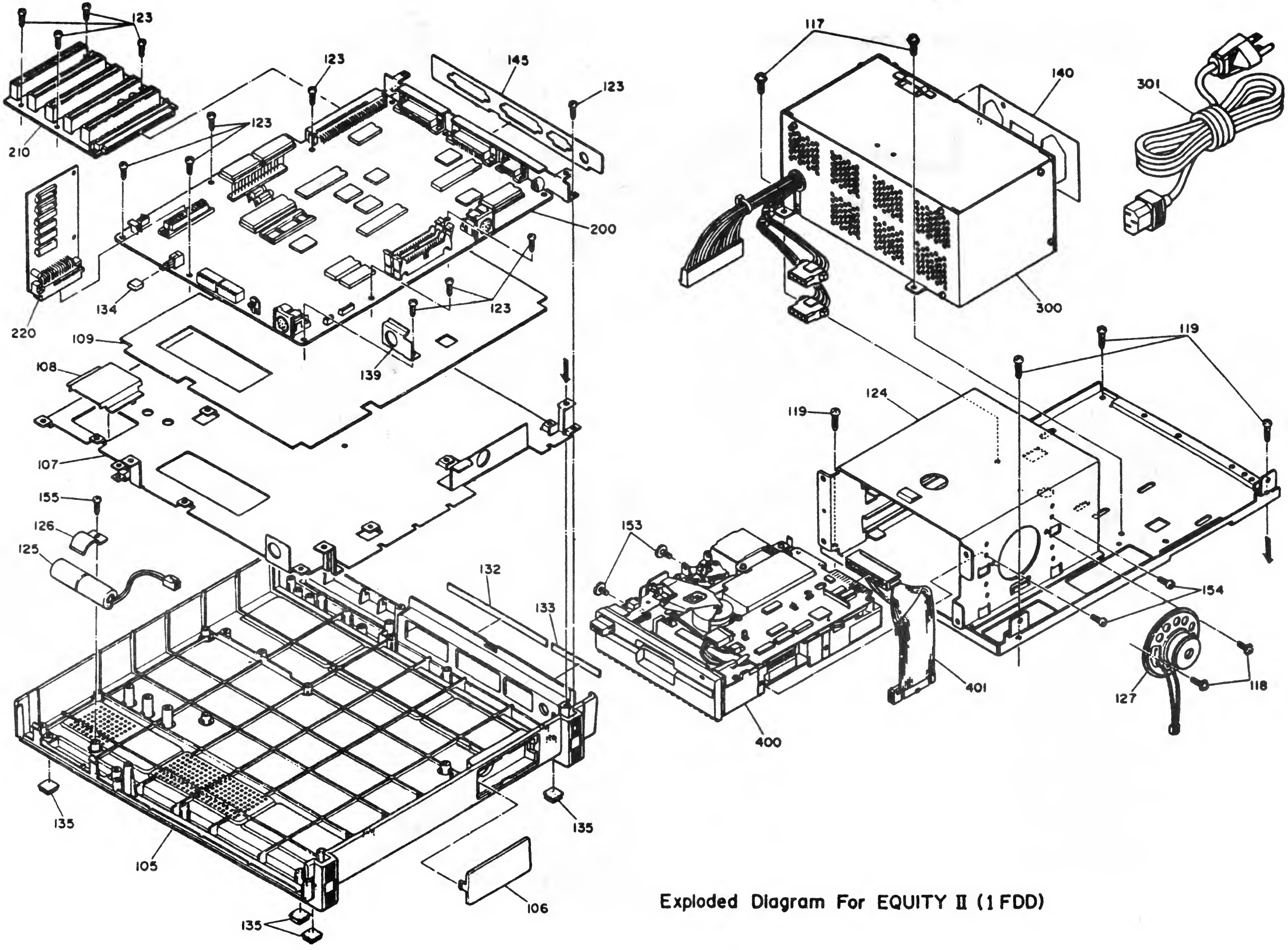
SECTION: PACKING MATERIALS (MAIN UNIT) **MODEL:** EQUITY II

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
02	Y147931001	INDIVIUAL CARTON BOX	1	6.21	
03	Y144933002	FRONT PACKING CUSHION	1	5.45	
04	Y144933003	REAR PACKING CUSHION	1	5.45	
05	X680024010	PLASTIC PROTECTIVE BAG	1	0.35	
06	Y422932003	POWER CORD PLASTIC BAG	1	0.25	

REF.NO.	PART NO.	DESCRIPTION	QTY.	UNIT PRICE	REMARKS
01	Y145931001	INDIVIDUAL CARTON BOX	1	2.66	FOR EQUITY I/II (USA)
03	Y145933101	PACKING CUSHION R	1	2.05	
04	Y145933102	PACKING CUSHION L	1	2.05	
05	Y145933103	CABLE HOLDER	1	3.20	



Exploded Diagram For EQUITY II (1FDD)



Exploded Diagram For EQUITY II (1 FDD)

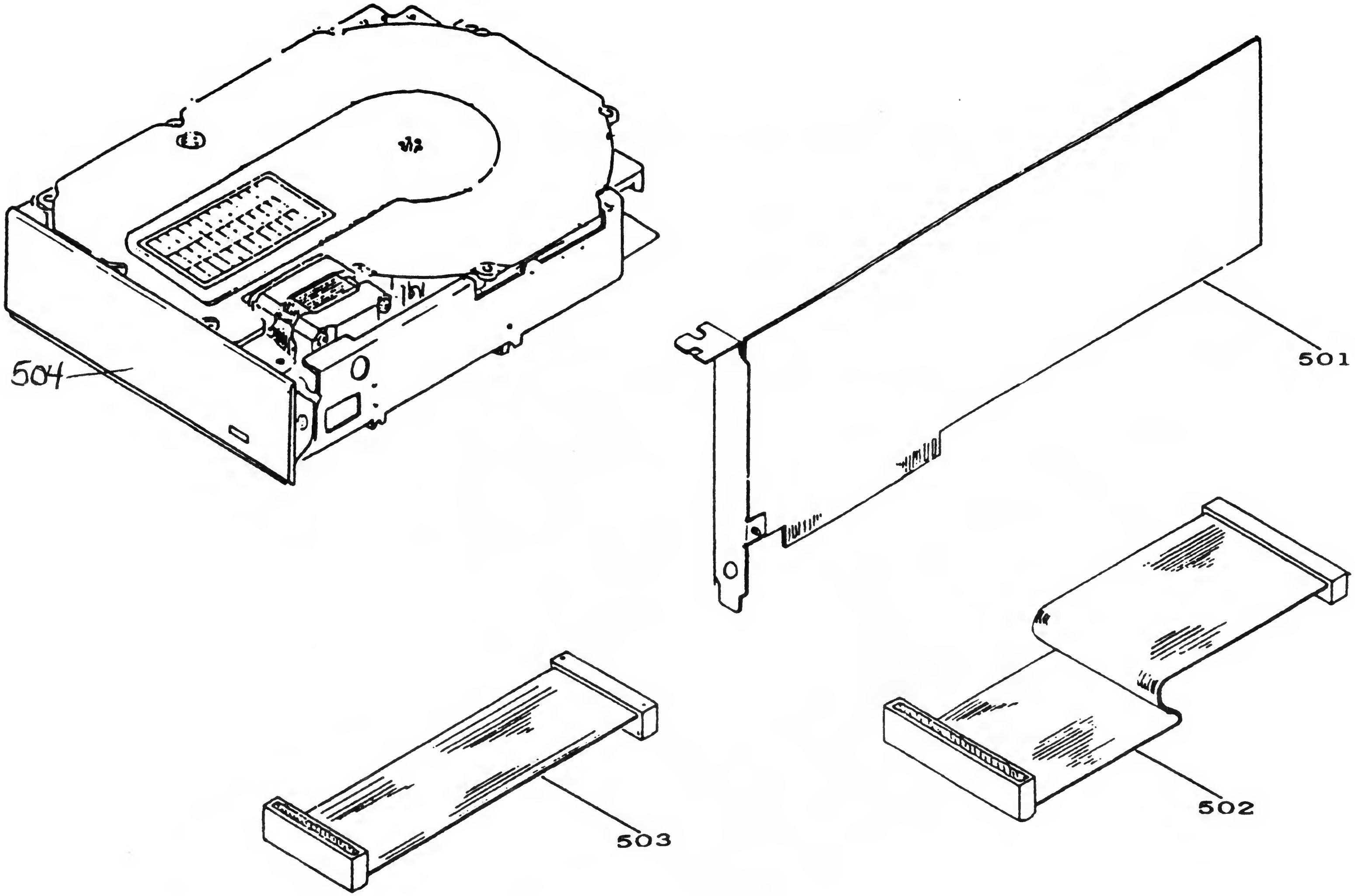
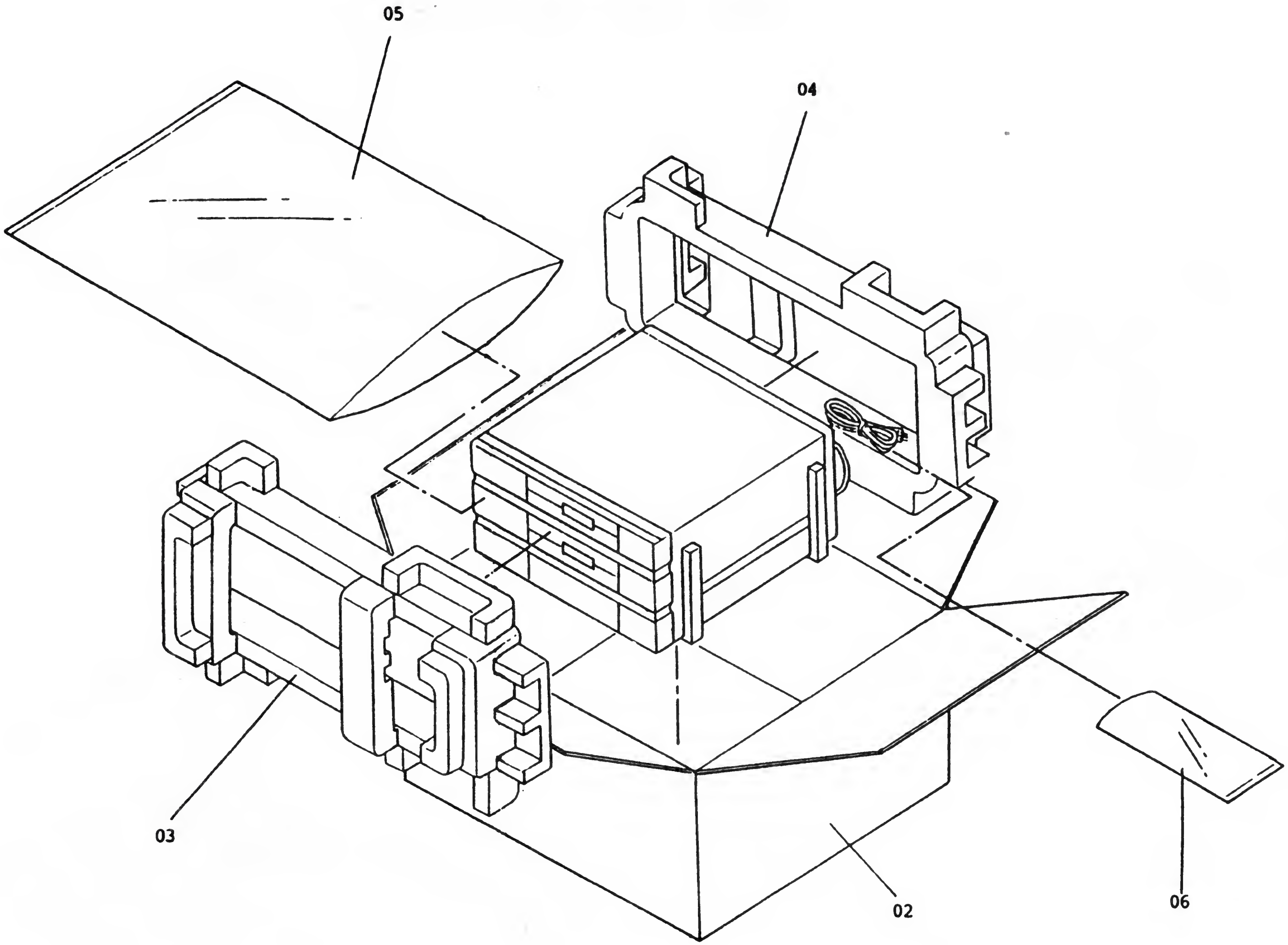
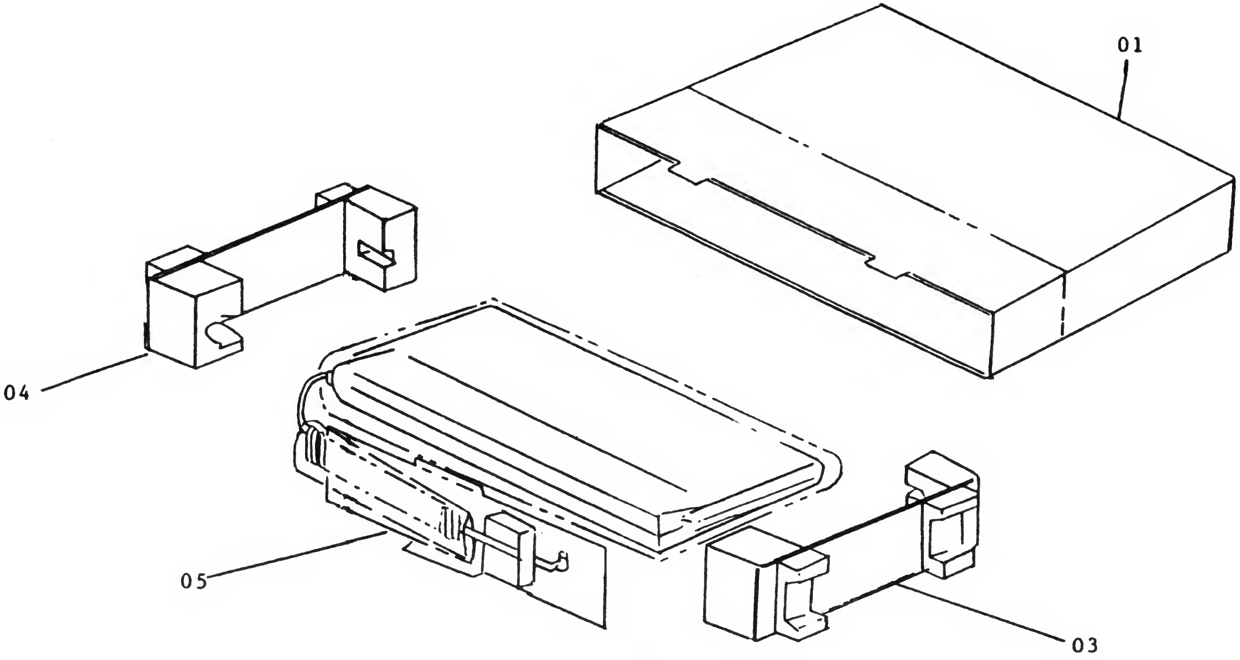


Diagram For HDD SET



EXPLODED DIAGRAM FOR PACKING MATERIALS FOR EQUITY-II



EQUITY I / EPSON PC
EQUITY II/ EPSON PC+

PACKING MATERIAL FOR KEY BOARD

BULLETINS

EPSON
SERVICE DIVISION

E P S O N
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/2/87 NUMBER: S-0001B
SUBJECT: EQUITY SERIES FDD/HDD COMPATIBILITY MATRIX

This document provides updated compatibility information on floppy disk drives, hard disk drives and hard disk controllers which have been supplied or are currently being supplied with the Equity series computers from Epson America, Inc.

The Equity I+, Equity II+ and Equity III+ computers have been included in this matrix.

Also included is information on which low level hard disk format procedures should be used with the various versions of hard disk controller boards.

Please refer to the Equity I, II, III IBM-PC COMPATIBLE HARDWARE/ SOFTWARE DIRECTORY supplied by Epson America's Marketing Department for information regarding third party floppy disk and hard drive compatibility.

EQUITY SERIES FLOPPY DISK DRIVE COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
360KB 5.25" FDD	I	I+	II	II+	III	III+	
MDD-531-51 (CANON)	X						
MD-5201-55 (CANON)	X						C
SD-525-501 (EPSON)	X						
MDD-531-31 (EPSON)			X		X		A,J
MD-5201-57 (CANON)		X	X	X	X	X	D,E
MD-5201-58 (CANON)		X	X	X	X	X	D,E,I
SD-521-506 (EPSON)		X	X	X	X	X	B
1.2MB 5.25" FDD	I	I+	II	II+	III	III+	
SD-580 (EPSON)					X		G
SD-581L-501 (EPSON)			X				B,F,G,H
JU-595-10 PANASONIC					X		
MD-5501-61 (CANON)				X	X	X	
FD1155C/FD1157C NEC				X	X	X	
720KB 3.5" FDD	I	I+	II	II+	III	III+	
SMD-489M (EPSON)		X	X	X	X	X	

COMMENT CODE EXPLANATIONS:

A. Requires insulating sheet when installed in lower position in Equity II. See TIB Equity II-006.
B. Jumper block SS1 - Position DS0 for drive A, DS1 for drive B
C. Equity I must have ROM BIOS version 2.21(MSA-B4) and MS-DOS 2.11 Release 1.04 or higher to use this drive.
D. Must set drive select jumpers on FDD logic board for A (position S1) or B (position S2).
E. It is not necessary to remove the terminating resistor pack.
F. Handle drive with care - possibility of short circuit between screw head on frame and FDD logic board (could damage FDD)!
G. Terminator must be removed when used as 2nd floppy drive unit.
H. See Product Support Bulletin S-0020 for set-up information.
I. Same as MD-5201-57 except comes configured as 2nd drive.
J. Jumper block JJ1 - Position S1 for drive A, S2 for drive B.

EQUITY SERIES HARD DISK DRIVE COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
20MB HARD DISK DRIVES	I	I+	II	II+	III	III+	
DK-505-2 (HITACHI)	X						C
HD-860-501/502/503	X	X	X				
HMD-720-802 EPSON	X	X	X		X		D
HMD-720-803 EPSON				X	X	X	
HD-860-504/505 EPSON	X	X	X	X	X	X	A, B
HD-860-506 EPSON	X	X	X	X	X	X	B
40MB HARD DISK DRIVES	I	I+	II	II+	III	III+	
D5146 (NEC)				X	X	X	
6053 (MINISCRIBE)				X		X	
94205-51 (CDC)				X		X	

COMMENT CODE EXPLANATIONS:

A. Comes with black front bezel.
B. When used with Equity III use format procedure #2 on page 5.
C. Follow format procedure #2 on page 5. The NCL Hard Disk Controller Board (NDC5027-49) and DK-505-2 HDD must be used together.
D. For Equity III - Only use HMD-720 hard drives NOT stamped with: "Do not use with Equity III".

EQUITY SERIES HARD DISK CONTROLLER COMPATIBILITY MATRIX

PRODUCT DESCRIPTION	COMPATIBLE WITH EQUITY MODEL						COMMENTS
HARD DISK CONTROLLER	I	I+	II	II+	III	III+	
WD1002S-WX2C027 ROM 62-000062-010	X						B,E
WD1002S-WX2C027 ROM 62-000062-010-1	X	X	X				B
WD1002A-WX1E027 ROM 62-000062-010-1 or 62-000062-13	X	X	X				B,C,D
NCL NDC5207-49	X						A
WD1002-WAH ROM 62-001020-10 AND 62-001027-11					X		
EPSON WHDC BOARD P/N Y127203000 ROM VERSION WD1015PL-27 or -27B 62-002008-011 or -061				X		X	F,G

CODE EXPLANATIONS:

A. Follow format procedure #2. NCL Hard Disk Controller Board (NDC5027-49) and DK-505-2 HDD must be used together

B. Follow format procedure indicated on PSB # S-0005.

C. Short version Western Digital HDC board. Released late 1986.

D. ROM BIOS 62-000062-010-1 and 62-000062-13 are equivalent. Either ROM may be found on this board.

E. This version HDC ROM BIOS with WD-1015-24 firmware CPU will not allow auto-boot from hard disk. WD-1015-14 firmware CPU will work.

F. ROM BIOS # WD1015PL-27 is equivalent to 62-002008-011 these ROMs have been updated to # WD1015PL-27B or 62-002008-061 which are also equivalent to each other.

G. HDC ROM BIOS must be revision "B" to work with XENIX software.

HARD DISK FORMATTING INFORMATION

```
*****IMPORTANT*************IMPORTANT*****************IMPORTANT******
*                                                                  *
*      ALWAYS FORMAT THE HDD WITH THE SAME VERSION CONTROLLER      *
*      BOARD AND HDC CPU FIRMWARE VERSION IT WILL BE USED WITH.    *
*      IT IS NOT NECESSARY TO REFORMAT IF THE ROM BIOS IS          *
*      UPGRADED AS LONG AS THE SAME FIRMWARE CPU IS USED.          *
*                                                                  *
********************************************************************
```

FOR LOW LEVEL FORMATTING:

1. EQUITY I/II FORMAT
   See PSB # S-0005 titled Equity I/II HDD intialization procedure using software which is included with each system.

2. EQUITY III FORMAT
   a. Run PFORMAT - Enter bad tracks - Time approx. 5 minutes.
   b. Run HDFMTALL - Time approx. 8 minutes.
   c. Run HDPART - Time approx. 2 minutes.
   d. Run HDFORMAT - Time approx. 5 minutes.

3. EQUITY III+ - See Product Support Bulletin # S-0006

Notes:

1. Early production Equity I units without HDDs must be upgraded with the CAC version VFO SUB-board to operate with a hard drive.
2. Equity I, DOS ver. 2.11 problem - Bad sector information erased when HDFORMAT (MS-DOS utility) executes formatting.
   Corrected in DOS version 2.2 (MSA-B3) and 2.21 (MSA-B4).
3. Equity I/II - HDFMTALL erases bad sector information.
   Delete HDFMTALL from the system disk.

EPSON

EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 2/4/87 NUMBER: S-0002
SUBJECT: USING THE PLUS DEVELOPMENT "HARDCARD" WITH EQUITY I/II

The Plus Development "HardCard" is a 20 megabyte fixed disk mounted on an expansion slot card, for use in IBM PC/XT and compatible computers. The unit employs controller circuitry from OMTI/Scientific Micro Systems, and uses 2,7 RLL encoding.

The HardCard has been found to be compatible with the Equity I and II computers, but there has been some confusion among customers who are running through the installation procedures. This is due to the HardCard's special installation procedure which has been designed specifically for use with PC-DOS. Because of certain file name differences between Epson's MS-DOS and IBM's PC-DOS, the Plus install program will not run using Equity MS-DOS.

Unfortunately, Plus Development does not officially support the use of the HardCard in the Equity computer series, because it has not been formally tested and approved by Plus Development. It has, however, been tested and officially approved by Epson's Vendor support staff.

The HardCard is shipped in a partitioned and formatted state, with a number of files included on it. The directory of files is as follows:

```
INSTALL   EXE    47479   1-01-80   12:06a
HCD       BAT       30   1-01-80   12:07a
HCD1      BAT      128   1-01-80   12:07a
HCD2      EXE    54769   1-01-80   12:07a
HCD3      DAT    13440   1-01-80   12:07a
HCD3      DIF      704   1-01-80   12:07a
HCD6      SCR     4224   1-01-80   12:07a
PREPARE   BAT      235   1-01-80   12:08a
SHELL     BAT       18   1-01-80   12:07a
LIGHT     COM      145   1-01-80   12:07a
SOUND     COM      145   1-01-80   12:07a
PATCHFMT  EXE    12670   1-01-80   12:08a
INSTALL   DAT      425   1-01-80   12:06a
```

These files comprise the installation routine (INSTALL.EXE, INSTALL.DAT, PATCHFMT.EXE, PREPARE.BAT, and SHELL.BAT), the Plus Development fixed disk menu program (HCD*.*), and supplemental utilities (LIGHT.COM and SOUND.COM).

Once the HardCard has been physically installed in the computer, the user boots the system with PC-DOS/MS-DOS (from the floppy drive), runs SYS.EXE (which is named SYS.COM on Equity MS-DOS) to transfer the O/S to the HardCard, then copies several DOS files to the root directory of C:. The user then invokes INSTALL.EXE which runs an 8-10 minute "hands-off" procedure that fully prepares the HardCard for use. This consists of partitioning and formatting, and loading their menu program and preparing it for auto execution.

For Equity "power users" who are comfortable with MS-DOS, and who don't wish to use the Plus-supplied menu program, they can set up the HardCard by simply copying the Plus files to a formatted floppy diskette, and then using HDPART and HDFORMAT in the normal fashion (Equity II users should run SETUP.COM first to make sure that drive C: is properly specified - for the HardCard, it should be set as "Not installed or other"). Users may want to copy the LIGHT.COM and SOUND.COM utilities back to the HardCard, as these files control visual and audible signals that are used to indicate HardCard access. The visual indicator is a flashing "+" sign at the upper right of the display (defaults to ON), and the audible indicator is a buzzing sound (defaults to OFF). However, if the user would like to set up the HardCard as though the Plus installation was performed (i.e. complete with their "shell"), then they should manually duplicate the Plus routine, as detailed in the following section. This procedure was outlined by the Plus Development technical staff, and I have substituted the alternate commands that the Equity MS-DOS uses.

Note that, while some of the steps seem redundant, the procedure was designed so that disk swapping on a single floppy system would be minimized, and also for automatic operation.

HARDCARD INSTALLATION - MODIFIED FOR EPSON EQUITY I/II

1. Boot the computer using the Epson MS-DOS disk (EQUITY II USERS ONLY: run SETUP.COM and set drive C: for "Not installed or others").
2. Enter SYS C: to transfer the operating system to the hardCard.
3. Copy COMMAND.COM and FORMAT.COM from the MS-DOS diskette into the root directory of the HardCard.
4. Remove the MS-DOS diskette and insert a blank diskette in drive A:. Log onto C: and enter FORMAT A: to prepare the blank diskette.
5. Copy all files from the HardCard to the formatted diskette. Label this diskette "Plus Utilities".
6. Remove the Plus Utilities diskette and press the RESET button on the Equity. The system should reboot from the HardCard.
7. Reinsert the Equity MS-DOS diskette (EQUITY II: insert the Equity GW-BASIC/UTILITIES diskette), log onto drive A: and run HDPART and HDFORMAT/S to partition and format the HardCard. When finished, remove the Equity diskette and reset the system. Ensure that the Equity boots from the HardCard.
8. Reinsert the Plus Utilities diskette. Copy all the files from the Plus Utilities diskette back into the root directory of the HardCard. Remove the Plus Utilities diskette and store in a safe place.
9. Copy all files from the Equity diskette(s) into the root directory of the HardCard.
10. Log into the root directory of drive C: and enter the command PREPARE. This will run a batch file that will create 16 empty subdirectories on the HardCard, into which applications software will later be loaded.
11. Also in this directory, rename the program SHELL.BAT to AUTOEXEC.BAT. This will cause the system to automatically load the Plus menu "shell" on bootup.12). Finally, erase PATCHFMT.EXE, PREPARE.BAT, and INSTALL.* from the root directory of C:.
12. The HardCard installation is now complete. Test the system by rebooting - the Plus menu "shell" should run.

NOTE: The original Plus install program creates a floppy diskette containing the Plus files, as above, but also performs several other operations to make it what they refer to as the "REINSTALL" diskette. This Reinstall diskette can later be used for reformatting of the HardCard. Using the modified Equity procedure, however, the "Plus Utilities" diskette that is created cannot be used as the Reinstall diskette. If an Equity user wants to reformat the HardCard, the user should use ARCHIVE to back up the contents, run HDFORMAT/S, then use ARCHIVE to restore the files.

EPSON

EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 2/6/87 NUMBER: S-0005
SUBJECT: EQUITY I/II HARD DISK INITIALIZATION

This is a basic guide for the installation and initialization of hard drives for the Equity I and II. Those of you that have the SPHDD.BAT may continue to use it; there are also a number of excellent third-party utilities, such as SpeedStor, that may be used. However, this method can used with just the systems software as provided with each machine.

1. Before physically installing the drive, either copy the information from the defect list on the top of the drive or make sure that you have the copy that was included with the drive. What you'll be needing is the cylinder/head information - you don't need the byte location.

2. Verify that the terminating resistor pack is installed and that the drive select jumper or switch is correctly set. The drive should be selected as the lowest number - i.e., DS0 assuming a range of DS0-DS3.

3. Some drive manufacturers do the physical or "low-level" format at the factory. DON'T ASSUME THIS! One indication is this: start the HDFMTALL program. If the cylinder count-down goes quickly (approx. 1 sec. per cylinder), thenthe physical format is very likely sound. If it takes longer than this, other measures are called for. Re-boot the system and proceed to step 4.

4. Invoke the DEBUG program. At the dash (-) prompt, enter: g=c800:5 and press ENTER. At this point, DEBUG executes (Goes to) the instructions at hex address c800, offset 0005. This is the ROM BIOS on the HD controller card. Stored at this address is the physical formatting routine provided by the controller manufacturer. You may encounter two types: Western Digital or National Computer Labs (NCL). The Western Digital is the simpler of the two. It presents you with information about how the drive number and interleave factor are stored in the AX register and prompts "Press y to begin formatting drive C with interleave 03". Press any key other than "y" and it aborts. If you enter "y", it IMMEDIATELY proceeds with the format. DON'T PRESS "Y" UNLESS YOU REALLY MEAN IT! It will then inform you when the format is complete and return you to the A prompt.

The NCL format is somewhat more complicated. It will ask you for drive number (0), number of cylinders (615), number of heads (4), reduced write current (615), write precompensation (615) and maximum ECC data error burst length (11). The numbers given here in parentheses would be typical for the HMD-720-802. It will then ask if all is correct; if yes, it proceeds with the format. If not, it returns you to the top of the input menu. In any case, when it completes the format, it may ask you if you wish to enter alternate track selections. Tell it "no".

5. Invoke the program HDFMTALL. This program will allow you to reconstruct the bad track table, which we just knocked out with the physical format. HDFMTALL will ask if you want a "standard" format; press "N". It will then ask if you want the default interleave of 3; you can accept this or change it. (I've found that an interleave of 6 seems to be pretty optimal on the I and II.) HDFMTALL will then display the bad track table and give you the chance to edit it. If any bad tracks are displayed, make sure that any bad locations from the error list you took off of the drive are indeed flagged. If not, enter them manually. If the scan turned up an excessive (more than 50) number of bad tracks, you might want to delete them and then manually enter the ones from the error list. Press "F" when you are finished and HDFMTALL will proceed with the warnings and then the actual format.

6. You're now ready to use HDPART. This program sets up the MS-DOS partition and writes the DOS file structure to the disk. Typically, you'll use the entire disk for DOS, so that simplifies matters. Just make sure that the DOS partition is specified as BOOTABLE. When you exit HDPART, the system automatically re-boots.

7. The final step - HDFORMAT. From the A prompt, enter the following: HDFORMAT C: /S/V. The /S switch transfers the operating system to the hard drive. The /V switch causes HDFORMAT to prompt you for a volume name for drive C. HDFORMAT now performs the logical format. When finished, remove the floppy from drive A and press CTRL-ALT-DEL. The system should boot from the C drive.

For those of you familiar with the IBM world, the DEBUG format is the same. HDFMTALL is the equivalent to IBM's Diagnostics level format; HDPART is our version of FDISK, and HDFORMAT is the same as IBM's FORMAT.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 3/16/87 NUMBER: S-0007
SUBJECT: EQUITY II PROBLEMS DUE TO IMPROPER DIPSWITCH SETTINGS

We would like to make you aware of a couple of different problems caused by improperly set dip switches on the Equity II computer.

Some customers have complained about Lotus 123 version 2.0 not running properly on the Equity II with the latest version ROM BIOS and MS-DOS.

The cause of the problems was determined to be that the co-processor switch (S1-2) was in the wrong position. It was switched "OFF" without a co-processor chip installed when it should have been in the "ON" position. After setting the switch correctly and rebooting the system the software ran normally.

This may also affect the operation of other software packages although we have not had any other reports.

Another problem was that after installing a hard drive in an Equity II the system displayed Drive D: instead of Drive C:. The problem was that the person who installed the hard disk drive forgot to reconfigure the dip switches for 1 floppy drive. This question has come up quite a few times.

***** CHECK THOSE DIP SWITCHES!! *****

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 6/8/87 NUMBER: S-0012
SUBJECT: EPSON EQUITY ENHANCED KEYBOARD COMPATIBILITY

The purpose of this bulletin is to provide information regarding the compatibility of the enhanced "AT" style Equity Plus series keyboard with the Equity family of computers and a general statement on software support.

With the introduction of the Equity I+ and III+, Epson brought out an enhanced keyboard design - very similar to the enhanced keyboard introduced by IBM on the Model 339 AT. There are a couple of areas to make note of.

1. Keyboard Compatibility

The enhanced keyboard cannot be used on an Equity I, II or III. The enhanced keyboard (as with IBM's) requires explicit ROM BIOS support. The Equity I+ and Equity III+ incorporate this support; the earlier machines do not.

It is possible, however, to use a third-party "enhanced-style" keyboard (such as the Datadesk Turbo-101) which offers switch selection for PC/XT or AT usage. (Please note that early versions of the Equity I and II did not support any third party keyboards.)

The correct jumper settings for non-Epson keyboards are:

Equity I:	J2 and J3 jumpered
Equity II:	J3, J4 and J5 set for position 1

Also note that once the above jumper changes have been made, attempting to use the Epson keyboard will result in damage to the keyboard and main board.

2. Software Compatibility

Not all applications "know" about the enhanced keyboard. The scan codes and mapping are subtly different. If you experience difficulties with certain applications (particularly any that re-program the keyboard), contact the software vendor and ask about enhanced keyboard support.

E P S O N
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 7/29/87 NUMBER: S-0014
SUBJECT: MS-DOS 3.2 AVAILABILITY FOR EQUITY I/II/III

The purpose of this bulletin is to provide information on the availability of MS-DOS 3.2 and the procedure for upgrading Equity I, Equity II and Equity III hard drive systems currently using earlier revisions of MS-DOS to the latest version of MS-DOS (Version 3.2).

MS-DOS 3.2 has been certified for use with the Equity I, Equity II and Equity III. This software is now available for users who wish to upgrade their system.

It can be ordered under Product Code Q395A-AA - $49.95 Retail. This package includes MS-DOS 3.2 and GW-BASIC software with documentation.

The following is a simple procedure to perform the transfer of the new MS-DOS 3.2 files to an existing hard disk system.

1. Insert the MS-DOS 3.2 diskette into drive A.
2. If the system is powered up, press RESET. If not, turn the system on.
3. At the A> prompt, type SYS C: and press ENTER. The system will respond with the message, SYSTEM TRANSFERRED.
4. At the A> prompt, type REPLACE A:\*.* C:\ /S and press ENTER. This will replace the existing MS-DOS files with version 3.2 files.
5. At the A> prompt, type REPLACE A:\*.* C:\[path] /A and press ENTER. This will copy new MS-DOS files to the subdirectory indicated by [path].
6. Remove the MS-DOS diskette and insert the GW-BASIC diskette into drive A.
7. At the A> prompt, type C: and press ENTER.
8. Repeat steps 4 and 5 above. (Prompt, listed in steps 4 and 5 as A>, will now be C>.)
9. Remove the GW-BASIC diskette from the drive. Put the original diskettes in a safe place for storage.

E P S O N

EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 7/29/87 NUMBER: S-0015A
SUBJECT: EPSON HD-860 HARD DISK DRIVE WARRANTY EXTENSION

The purpose of this bulletin is to inform you of a change in the warranty period for the HD-860 hard disk drive unit.

Epson America, Inc. has made the decision to extend the warranty period for the HD-860 hard disk drive, installed in the Equity product line, for an indefinite period. This warranty extension will cover all HD-860 hard disk drives regardless of the purchase date. Standard warranty claim procedures are to be followed for these failures. The normal warranty labor reimbursement and no charge parts exchange will be given for these claims.

This warranty extension is for HD-860 failures only and Epson America, Inc. reserves the right to cancel this HD-860 warranty extension at any time. It is designed to promote the satisfaction of our mutually inclusive customer base with the Epson products.

Epson's Service Department is currently providing HMD-720 hard disk drive units as warranty replacements for returned HD-860's. Authorized Service Centers and Customer Care Centers should not use HD-860's as repair replacements. Any ASC or CCC having HD-860's in repair float stock may exchange these for HMD-720's by contacting Warranty Administration for an RMA.

Note: This exchange does not apply to sales product, and is contingent upon availability of Epson's float exchange stock.

E P S O N
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 08/25/87 NUMBER: S-0017
SUBJECT: Equity Computers and Floppy Disk Drives

There is still some confusion regarding which FDDs will work with which Equity. Here is a quick reference for FDD selection (for detailed information, refer to PSB Number S-0001A).

Equity I	Epson Q520A-AA (360 KB)[1]
Equity I+	Epson Q213A-AA (360 KB) Epson Q112A-AA (720 KB 3.5")*
Equity II	Epson Q213A-AA (360 KB) Epson Q911A-AA (1.2 MB)[2]
Equity III	Epson Q213A-AA (360 KB) Epson Q212A-AA (1.2 MB)
Equity III+	Epson Q213A-AA (360 KB) Epson Q212A-AA (1.2 MB) Epson Q112A-AA (720 KB 3.5")*

1 - This is the *only* FDD compatible with the Equity I

2 - This is the *only* 1.2 MB FDD compatible with the Equity II

* - The Q112A-AA 3.5" FDD is scheduled for late September/early October delivery

One of the key issues is: NEVER USE ANY 1.2 MB FDD OTHER THAN THE Q911A-AA IN THE EQUITY II! The interface is slightly different from the AT "standard". As a result, an AT-type drive will work erratically (if at all). One of the problems is a disk change error, or continuing to use the directory from a previous disk.

Also on the Equity II, MS-DOS 3.2 does not allow sufficient retries on diskette read/write with the Q911A-AA. Consistent "Abort, retry, ignore?" messages result when attempting to log a new disk. Typically, "r" for retry will overcome this situation. MS-DOS 3.2 operation with the Q213A-AA is correct.

PRODUCT SUPPORT BULLETIN

DATE: 12/2/87 NUMBER: S-0019B
SUBJECT: EQUITY SERIES/APEX MATH CO-PROCESSOR SELECTION GUIDE

The purpose of this bulletin is to assist in selecting the appropriate numeric co-processor for use in the Epson Equity series computers and the Epson Apex computer.

Use the following table to determine which type of Numeric Co-Processor is recommended for the corresponding computer.

EPSON COMPUTER	CPU SPEED	NUMERIC CO-PROCESSOR	NXP SPEED
Equity I	4.77MHz	8087	5 MHz
Equity I+	4.77/10MHz	8087-1	10 MHz
Equity II	4.77/7.16MHz	8087-2	8 MHz
Equity II+	8/10MHz	80287-8	8 MHz
Equity III	6/8MHz	80287-6	6 MHz
Equity III+	6/8/(10/12)MHz*	80287-8	8 MHz
Apex	4.77/8MHz	8087-2	8 MHz

* Product enhanced with increased CPU speed of 6/8/12Mhz starting with all units manufactured in the U.S.A..

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 9/30/87 NUMBER: S-0020
SUBJECT: EQUITY II - 1.2MB FLOPPY DISK DRIVE INFORMATION

After installing MS-DOS 3.2 on the Equity II hard disk drive, whenever the 1.2MB floppy disk drive is accessed after booting from the hard disk the following error message is generated: "DISK READ ERROR ABORT, RETRY, IGNORE?"

This can be corrected by using the following line in the CONFIG.SYS file: DRIVPARM=/D:ddd /F:1

Only the Epson (Model Code Q911A-AA) 1.2MB FDD is compatible with the Equity II. The interface is slightly different from the AT "standard". As a result, an AT-type drive will work erratically (if at all). Problems which may occur when using other drives is a disk change error, or continuing to display the directory from the previous disk.

Subject: Equity II – 1.2MB Floppy Disk Drive Information

Date: 11/10/89
Page: 1 of 1

PSB No: S-0020A
Originator: REM

After installing MS-DOS 3.2 on the Equity II hard disk drive, whenever the 1.2MB floppy disk drive is accessed after booting from the hard disk the following error message is generated: "DISK READ ERROR ABORT, RETRY, IGNORE?"

This can be corrected by using the following line in the CONFIG.SYS file:

```
DRIVPARM=/D:d /F:1
```

d = 0 if the drive is installed as drive A:
d = 1 if the drive is installed as drive B:

Note: Only the Epson (Model Code Q911A-AA) 1.2MB FDD is compatible with the Equity II. The interface is slightly different from the AT "standard". As a result, an AT-type drive will work erratically (if at all). Problems which may occur when using other drives is a disk change error, or continuing to display the directory from the previous disk.

EPSON

EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 11/3/87
SUBJECT: EQUITY I/II PATCH PROGRAMS

NUMBER: S-0024

The purpose of this bulletin is to provide information on the availability of patch programs which have been developed to overcome some compatibility problems which may occur with a few application programs on the Equity I and Equity II computers.

These programs are available from the Epson America Inc. Service Department, Product Support - Systems Group on diskette.
The patch disk files (PATCH.ARC) can also be downloaded from the Epson Product Support RBBS system and from Compuserve's Epson Forum, they are compressed and can be uncompressed with ARC.

The Product Support RBBS system can be accessed 24 hours/day - 7 days/week by remote modem at Tel. (213) 534-8506.

Protocol: no parity, 1 stop bit, 8 data bits, 1200/2400 Baud.

The following is a list of the files which comprise the Patch disk:

```
AUTOEXEC.BAT
COMPOSIT.BAT
COMPOSIT.MOD
EGAN-PAT.ASM
EGAN-PAT.COM
EQRAMDVR.DOC
EQRAMDVR.SYS
FIXRPORT.ASM
FIXRPORT.COM
FLOPPY  .BAS
GOLDCARD.BAT
GOLDCARD.MOD
HARDISK .BAS
HERCDUMP.ASM
HERCDUMP.COM
HGC     .COM
HGC     .DOC
MATHBLAS.DOC
MODE    .COM
MODE    .DOC
MODEHERC.COM
MODEHERC.DOC
MUSTREAD.DOC
PATCHES .TXT
PATCHES2.TXT
PATCHES3.TXT
PSHERC  .ASM
PSHERC  .COM
READYPAT.ASM
READYPAT.COM
ROMPATCH.COM
ROMPATCH.DOC
VPHERC  .COM
VPREAD  .ME
```

The disk contains patch programs and documentation (TXT and DOC) files which are also contained in this Product Support Bulletin.

A detailed explanation of each patch program and their use is explained on the following pages.

FOR EQUITY I:

COMPOSIT.BAT - Modifies DU.EXE, SETUP.EXE, ARCHIVE.EXE and HDSIT.EXE to improve the brightness of messages when using a composite monitor.

GOLDCARD.BAT - Modifies DU.EXE, SETUP.EXE, ARCHIVE.EXE, SETPRINT.EXE and XTREE.EXE so they will run with the QUADRAM Goldcard with the Keysaver enabled.

EQRAMDVR.SYS - For those RAM DISK utilities which need it, an "empty" space disk drive is created. (See pages 6 and 7 for instructions on installing and using this file.)

ROMPATCH.COM - Equity I systems with ROM BIOS versions earlier than 2.20 will require this patch to increase the stack space in order to run certain application programs (Lotus 1-2-3 Version 2, for example). (See page 9 for instructions on installing and using this file.)

READYPAT.COM - Allows screen dump to take place while Living Videotext's READY! is loaded.

MATHBLAS.COM - Allows Math Blaster to run correctly. (See page 5 for instructions on using this file.)

PSHERC.COM - Allows Print Shop to run in Hercules graphics mode. Run PSHERC.COM before loading Print Shop.

EGAN-PAT.COM - Allows use of Honeywell's PC VIP terminal emulation software._

FOR EQUITY II

ROMPATCH.COM - Equity II systems with ROM BIOS versions earlier than 1.11 will require this patch to increase the stack space in order to run certain application programs (Lotus 1-2-3 Version 2, for example). (See page 9 for instructions on installing and using this file.)

MODE.COM - The supplied version of MODE did not function properly when used to switch from color to monochrome display (MODE MONO); this version does. MODE.COM is a modified version of the Equity II MODE utility. The MODE utility supplied with the Equity II will not work properly in the following configuration:

Internal video: Set to monochrome mode with monochrome monitor attached.

External video: IBM Enhanced Graphics Adapter (or equivalent) installed with color monitor attached.

Using the MODE utility to switch from color to monochrome display (MODE MONO) will freeze the cursor in one position on the monochrome display, or the cursor will disappear completely. The modified MODE utility will fix this problem. It will work exactly the same as the normal MODE utility in all situations, even when the IBM EGA adapter (or equivalent) is not installed.

MODEHERC.COM - RAM-resident utility which allows the use of Hercules monochrome graphics. MODEHERC.COM allows programs such as Lotus 123 release 1A to use Hercules emulation on the Equity II. These programs require that you run the Hercules utility HGC.COM (usually HGC FULL) to be able to utilize graphics.

SuperCalc 3 exhibits a different problem. It will display one graph successfully, then subsequent graphic displays will be garbled. MODEHERC.COM will also fix this problem.

Since MODEHERC.COM remains resident in memory, it only needs to be run once. It is recommended that MODEHERC.COM be the last memory resident program loaded on the system. For example, if you will be using Sidekick, run MODEHERC after Sidekick has been loaded into memory.

EQUITY II PATCHES (continued)

HGC.COM - Epson utility which allows the use of Hercules monochrome graphics. (See page 8 for instructions on installing and using HGC.COM.

PSHERC.COM - Allows Print Shop to run in Hercules graphics mode. Run PSHERC.COM before loading Print Shop.

EGAN-PAT.COM - Allows use of Honeywell's PC VIP terminal emulation software.

HERCDUMP.COM - Allows screen dump in Hercules Graphics mode. It is a memory resident program used in conjunction with GRAPHICS. The GRAPHICS program must be run first.

VPHERC.COM - Allows VP Planner to work in Hercules mode.

READYPAT.COM - Allows screen dump to take place while Living Videotext's READY! is loaded.

HGC.COM - Epson utility which allows the use of Hercules monochrome graphics. (See page 8 for instructions on installing and using HGC.COM.)

FIXRPORT.COM - Program to let Lotus Report Writer use Equity II Color mode. Report Writer apparently forces the Equity II into monochrome video mode even when a color video adapter is attached.

MATHBLAS.COM INSTALLATION

Math Blaster is an educational game produced by Davidson and Associates in Torrance Calif. It works well with the entire Equity series except the Equity 1 running color mode. The large numbers that Math Blaster places on the screen are done in graphics mode. These numbers appear as square blocks of garble on the Equity 1 color screen. Unlike the GWBASIC used on the Equity II and III, GWBASIC for the Equity 1 does not initialize certain memory areas. In particular, area 510 of segment 0 is not initialized (this area is used by BASIC to hold the default data segment value).

Tests have been run on ROM BIOS versions 2.1i, 2.20 and 2.21. The following programs have proved to be an effective fix for cases tested so far:

HARDISK.BAS - For hard disk versions:

```
10 PRINT " This patch will not work with config.sys files"
20 DEF SEG =0
30 POKE &H510,&HC9
40 POKE &H511,&H14
50 RUN "color
```

FLOPPY.BAS - For Floppy disk versions.

```
10 DEF SEG =0
20 PRINT "this is a fix for the floppy disk system"
30 PRINT "make sure no CONFIG.sys file is active"
40 PRINT "try this version on floppy systems"
50 POKE &H510,&HC3
60 POKE &H511,&H14
70 RUN "color
```

CONFIG.SYS and AUTOEXEC.BAT move things around in memory. These patch programs will not work if either of these two programs are activated on boot up.

Please copy the appropriate program to the disk that contains your Math Blaster program. Run these programs and they will run the Math Blaster program for you.

WHY AND HOW TO USE EQRAMDVR.SYS

Many RAM disk programs supplied with expansion boards do not work with an Equity I with dual floppy disks. The Equity I supports only two floppy disk drives, and these programs expect the operating system to treat it as a floppy disk. RAM disk utilities that are in device driver form (must be specified in CONFIG.SYS) should have no problems. Any RAM disk utility that is executed from the system prompt will have problems on a dual floppy Equity. These are the programs EQRAMDVR.SYS was designed to support. The device driver EQRAMDVR.SYS provides the support needed for these utilities by creating an 'empty' disk drive that a RAM disk program can use when it is executed.

HOW TO USE EQRAMDVR.SYS

Since EQRAMDVR.SYS is a device driver, it must be specified in the CONFIG.SYS file on your boot disk. See pages 3-1 to 3-4 in "MS-DOS for the Equity I" for a description of the CONFIG.SYS file. The boot disk can either be a floppy disk or a hard disk. The file EQRAMDVR.SYS must also be copied to your boot disk. In the following instructions, [ENTER] means press the ENTER key, and [F6] means press the F6 key.

1. Boot your system with your working copy of MS-DOS. If you have a hard disk that is set to autoboot, boot from the hard disk.

2. When the MS-DOS prompt appears, place the disk with EQRAMDVR.SYS in drive B: (A: for hard disk systems).
   For a floppy disk system, type:COPY B:EQRAMDVR.SYS [ENTER]
   For a hard disk system, type: COPY A:EQRAMDVR.SYS [ENTER]

3. Check if CONFIG.SYS already exists on your boot disk by typing: DIR CONFIG.SYS [ENTER]
   If the message "File not found" appears, follow step 4a, otherwise follow 4b.

4a. Type:
```
COPY CON: CONFIG.SYS [ENTER]
DEVICE=EQRAMDVR.SYS /2 [ENTER]
[F6] [ENTER]
```

4b. Type:
```
COPY CONFIG.SYS + CON: CONFIG.SYS [ENTER]
DEVICE=EQRAMDVR.SYS /2 [ENTER]
[F6] [ENTER]
```

Note: The /2 above is optional. It will be explained in the following section.

5. Reset the system, and your Equity I is now ready to use a RAM disk program.

EQRAMDVR.SYS OPTIONS AND OPERATION

There is one option for EQRAMDVR.SYS. Typing a /n (where n is a number from 1 to 4) after DEVICE=EQRAMDVR.SYS sets the number of RAM disks that can be supported. In the instructions above, the /2 will allow the Equity I to support two RAM disks. If the /n option is omitted, EQRAMDVR.SYS sets up support for one RAM disk.

When the system boots, EQRAMDVR.SYS will display a sign on mesage similar to this:

```
RAM disk emulator support installed at drive(s) C:, D:
```

There will from one to four drive letters shown, depending on the /n option. When you execute your RAM disk program, be sure to use the drive letter shown in the sign on message. For example, using Tecmar's MEMDISK program, you would type this command at the MS-DOS prompt:

```
MEMDISK D: -BUF160
```

This would set up a 160K RAM disk at drive D:.

If you attempt to use one of the EQRAMDVR.SYS drives before running your RAM disk program, you will get one of the following error messages:

```
Not ready error reading drive x
Abort, Retry, Ignore?
```

or

```
Bad command  error reading drive x
Abort, Retry, Ignore?
```

The x would actually be the letter of the drive you tried to access. Press A to abort, then run your RAM disk program.

HGC.COM INSTALLATION

The Equity II offers Hercules compatible graphics. In order to use Hercules modes with certain applications, for example Lotus 123 release 1A, you must select "HGC FULL" and for Enable V2.0 you must select "HGC HALF" with the program HGC.

The program HGC.COM is designed to act like the Hercules Graphics utility of the same name. It supports three commands, which must be on the command line after program name:

DIAG - Enter diagnostic mode (IBM monochrome mode 7 compatible). Type: HGC DIAG

HALF - Enter half-memory mode. This enables Hercules graphics for page 0 at b0000-b8000. Type: HGC HALF

FULL - Enter full-memory mode. This enables Hercules graphics for both pages 0 at b0000-b8000 and 1 at b8000-c0000. Type: HGC FULL

Note: 1. Commands may be upper or lowercase.
2. This version does not support the SAVE command.

VP PLANNER PATCH

SYSTEM: EQUITY II HERCULES MODE

VPHERC.COM is a TSR (MEMORY RESIDENT) program which enables VP PLANNER to function properly when running on the Equity II configured for HERCULES video support. Run VPHERC before running VP PLANNER. It is suggested that you make a batch file in order to accomplish this.

ROMPATCH INSTALLATION INSTRUCTIONS

Some Equity I and Equity II computers have trouble running certain application programs (Lotus 1-2-3 Version 2, for example) because they have an early version of ROM BIOS. This diskette contains a patch named ROMPATCH.COM which either corrects the problem (by patching the ROM) or tells you that your computer does not need it.

Follow the instructions below to install the patch if you have an Equity I or an Equity II.

Installing the Patch

At the MS-DOS system prompt, type: ROMPATCH and press Enter. One of the following messages appears:

```
Resident portion of ROMPATCH version 1.0 loaded
```

This indicates that the patch was necessary and has been properly installed in the lowest available memory. If you see this message, you need to install this patch every time you load MS-DOS. You may want to include ROMPATCH in your AUTOEXEC.BAT file, so it is installed automatically every time you boot your Equity. (See your MS-DOS manual for instructions on creating an AUTOEXEC.BAT file.)

```
ROMPATCH version 1.0 already installed
```

This indicates that ROMPATCH.COM has already been properly installed since you last booted your Equity.

```
No need to install ROMPATCH version 1.0
```

This indicates that your Equity's ROM BIOS does not need the patch and you can disregard this patch and these instructions.

If your system does need the patch, remember to install it each time you boot your Equity or include it in your AUTOEXEC.BAT file.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/3/87 NUMBER: S-0027
SUBJECT: Equity II and III with the Epson 3.5" Floppy Drive

The Equity II and III have been tested with the new Epson 3.5" floppy disk drive (A112A-AA). The purpose of this bulletin is to detail the proper procedure for installation and configuration.

1. The Equity must be upgraded to MS-DOS 3.2 (Q395A-AA).

2. The appropriate DRIVPARM command must be added to the CONFIG.SYS file. This defines the correct parameters for block devices (such as disk drives) under MS-DOS. While there are a number of switches to the DRIVPARM command, only two concern us: the logical drive number and the form factor index. For example, to set up the drive as B, add the line:

   ```
   DRIVPARM = /D:1 /F:2
   ```

   to the CONFIG.SYS file. This establishes it as the second logical drive with a 720KB form factor index. The /D: value should be 0 for drive A.

3. The drive must be physically selected, as well. You will find a shorting block designated SS1 on the drive. If installed as A, the jumper should be installed on D0. For drive B, install it on D1.

4. The cable configurations are different between the Equity II and the Equity III. For the Equity II, for drive A, use the cable from connector CN9 on the main board. For B, use CN10.
   On the Equity III, use the center cable connector for A and the end connector for B.

For more information on the DRIVPARM command, please refer to the chapter "*Configuring Your System*" in the MS-DOS 3.2 manual.

EPSON
EPSON AMERICA INC.
SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/3/87 NUMBER: S-0028
SUBJECT: EPSON 3.5" 720KB FLOPPY DISK DRIVE COMPATIBILITY

The purpose of this bulletin is to provide information regarding the compatibility of the Epson 3.5", 720KB floppy disk drive (Product Code A112A-AA) with the Equity series computers and Apex computer.

The 3.5" floppy disk drive must be used with MS-DOS 3.2 or higher.

The Epson 3.5" floppy disk drive has been tested and found to be compatible using MS-DOS 3.2 in the following systems:

Apex	No special setup required
Equity II	Must include DRIVPARM in CONFIG.SYS
Equity III	Must include DRIVPARM in CONFIG.SYS
Equity I+	No special setup required
Equity II+	No special setup required
Equity III+	No special setup required

The 3.5" floppy disk drive is not compatible with the Equity I.

Refer to Product Support Bulletin # S-0027 for detailed information on using the DRIVPARM command to configure Equity II and Equity III systems for using the 3.5" floppy disk drive.

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SERVICE DEPARTMENT

PRODUCT SUPPORT BULLETIN

DATE: 12/18/87 NUMBER: S-0032
SUBJECT: Using Lap-Link with the Equity II

This bulletin describes a problem we've identified in using the Lap-Link data transfer program from Traveling Software with the Equity II computer.

Lap-Link is supplied with the Equity LT laptop computer and is also widely used with other laptop PCs.

Lap-Link transfers data via the serial ports of the two PCs using a direct-connect cable. It operates at a very high baud rate - in fact, it defaults to 115,200 bits per second. The Equity II's built-in serial port will not operate at speeds faster than 57,600 bps. If you attempt to load Lap-Link with its default settings on an Equity II, the system will simply lock up, forcing a reset.

The first (and easiest) way of dealing with this situation is to configure Lap-Link on a different system. You cannot reconfigure Lap-Link on the Equity II because it locks up before you can change the settings. Load the working copy of Lap-Link on another PC, select Options, cursor over to Baud and then cursor over to 57600. Select Save from the Options command line and enter Y to the "Ok to save settings?" prompt. You now have a version of Lap-Link that will work correctly on the Equity II. Please note that you will have to set the baud rate on the other system to match.

If you have access to an option card with a serial port, you can use it to re-configure Lap-Link. Set DIP switch 2-8 on the front panel of the Equity II to the ON (or UP) position to disable the internal port. Set the option card port as COM1 and install the card. You may then either use the port on the card permanently at 115,200 bps or configure Lap-Link down to 57,600 bps, remove the card and re-enable the internal port.

This problem exists with all versions of the Equity II system boards.

Once properly configured, you'll find Lap-Link to be a great help in moving data between different systems.

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ENGINEERING CHANGE NOTICE

E C N NO. : EQII-001
DATE : 08/29/86
MACHINE (s) : EQUITY II
PAGE (s) : 1 of 1
SUBMITTED BY: Sid Arzu
REFERENCE : ES 86-0080
AUTHORIZED BY :

TITLE: EQUITY II OPTIONAL 360KB FDD TERMINATOR REMOVAL

APPLICABILITY

All Equity II optional 360KB floppy disk drives.

DATE OF CHANGE

From July 1986.

MODIFICATION

The terminator resistor pack has been removed from the FDD Main Circuit Board Unit of optional FDD kits.

REASON

A second floppy disk drive (drive "B") with a terminator resistor pack may not operate reliably and can cause damage to the MCY Board.

ACTION REQUIRED

When installing a second floppy disk drive in the Equity II, ensure that the terminator resistor pack has been removed.

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ENGINEERING CHANGE NOTICE

ECN NO.: EQII-002
DATE: 02/13/87
PAGE (s): 1 of 1
SUBMITTED BY: John DeBenedetti
AUTHORIZED BY:

MACHINE (s): EQUITY II
REFERENCE: SB Q-138

TITLE: Equity II ROM BIOS EPROMs upgrade to MASKED ROMs

DATE OF CHANGE:

December, 1986

SERIAL NUMBERS AFFECTED:

Not available

MODIFICATION:

The ROM BIOS EPROMS have been changed to MASKED ROMs

REASON:

To maintain a constant parts supply

ACTION REQUIRED:

None

PART NUMBER CHANGES:

Location	Current	New
5U	2764 MQA-A2 Y147800702	M5M2764P-311 MSA-A2 Y147810702 (Masked ROM)
4U	2764 MQA-B2 Y147800802	M5M2764P-311 MSA-B2 Y147810802 (Masked ROM)

INTERCHANGEABILITY:

Current and new parts are interchangeable.

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ENGINEERING CHANGE NOTICE

ECN NO.: EQII-003
DATE: 6/24/87
PAGE (s): 1 of 1
SUBMITTED BY: John DeBenedetto
AUTHORIZED BY:

MACHINE (s): EQUITY II
REFERENCE: SB Q-187

TITLE: EQUITY II FDD FIXING PLATE MODIFICATION

DATE OF CHANGE:

Not available

SERIAL NUMBERS AFFECTED:

Not available

MODIFICATION:

The FDD fixing plate has been modified as follows:

1. The new fixing plate requires only 1 screw to fasten the speaker. The old one required 2 screws.
2. The FDD propping tab has been eliminated on the new fixing plate.

REASON:

To improve serviceability

ACTION REQUIRED:

None

PART NUMBER CHANGES:

Current	New
(Y144018002)	(Y144018003)

INTERCHANGEABILITY:

Current and new parts are interchangeable.

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ENGINEERING CHANGE NOTICE

E C N NO. :	EQII-004
DATE :	6/24/87
MACHINE (s) :	EQUITY I/II
PAGE (s) :	1 of 2
SUBMITTED BY:	John DeBenedetti
REFERENCE :	SB Q-169
AUTHORIZED BY :	

TITLE: MODIFICATION OF BOTTOM COVER FOR EQI / EQ II

DATE OF CHANGE:

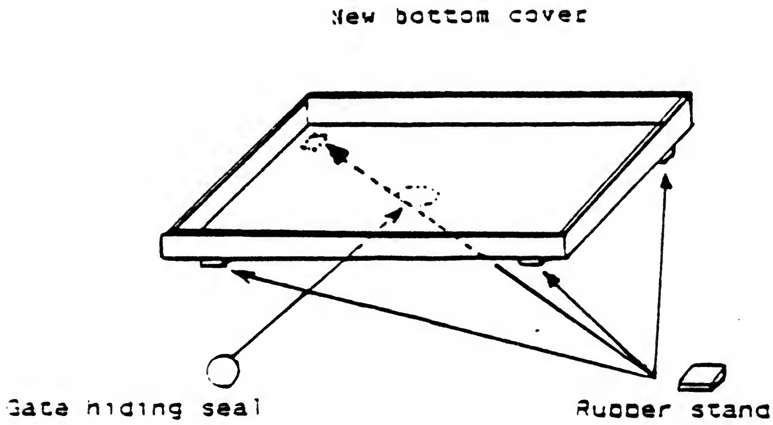
May 14, 1987

SERIAL NUMBERS AFFECTED:

Not available

MODIFICATION:

The bottom cover for the EQ I and II has been changed. The new cover comes without the rubber stands and gate hiding seal.



REASON:

To maintain a constant parts supply.

NO.: EQII-004
DATE: 6/24/87
PAGE: 2 of 2

ACTION REQUIRED:

When ordering the bottom cover always order the rubber stands (Y144008000) and the gate hiding seal (Y144506001) also.

PART NUMBER CHANGES:

	Current	New
Bottom Cover	Y144000001	Y144000201

INTERCHANGEABILITY:

Current and new parts are interchangeable.

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ENGINEERING CHANGE NOTICE

E C N NO. : EQII-005
DATE : 6/24/87
PAGE (s) : 1 of 1
SUBMITTED BY: John DeBenedetti
AUTHORIZED BY :

MACHINE (s) : EQUITY I/II

REFERENCE : SB Q-170

TITLE: REMOVAL OF JUMPER CONNECTOR PINS FROM WD1002A-WX1E027 HDC

DATE OF CHANGE:

May 14, 1987

SERIAL NUMBERS AFFECTED:

Not available

MODIFICATION:

The jumper connector pins W-5 and W-7 are removed from the Western Digital Hard Disk Controller WD1002A-WX1E027. The connections are hard jumpered on the board.

REASON:

To facilitate manufacturing

ACTION REQUIRED:

None

PART NUMBER CHANGES:

None

INTERCHANGEABILITY:

Current and new boards are interchangeable.

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TECHNICAL INFORMATION BULLETIN

T I B NO.: EQUITY II-001
DATE: 12-06-85
PAGE (s): 1 of 1
SUBMITTED BY: Sidney Arzu
AUTHORIZED BY:

MACHINE (s): EQUITY II
REFERENCE: NONE

TITLE: EQUITY II OPTION SLOT POWER AVAILABILITY

The following information is provided to assist in determining the current available to the option board (MCY-MT) plug-in card slots. A breakdown is given for each of four configurations of the EQUITY II system as follows:

1. Configuration A: One (1) 360KBytes FDD, 640KB RAM.
2. Configuration B: Two (2) 360KBytes FDD, 640KB RAM.
3. Configuration C: Two (2) FDD's (one 360KB and one 1.2MB), 640KB RAM.
4. Configuration D: One (1) 360KB FDD, one (1) HD-860 One (1) HDD Controller, 640KB RAM.

OPTION SLOTS CURRENT AVAILABLE (MAXIMUM)
VERSUS SYSTEM CONFIGURATION

POWER SUPPLY VOLTAGE	A	B	C	D	PIN NO.
+ 5 V	5.15 Amp.	4.92 Amp.	4.03 Amp.	3.84 Amp.	B3, 29
+12 V	4.00 Amp.	3.65 Amp.	3.65 Amp.	3.05 Amp.	B9
- 5 V	300 mA.	300 mA.	300 mA.	300 mA.	B5
-12 V	300 mA.	300 mA.	300 mA.	300 mA.	B1, 10

The total current draw of all option cards should not exceed the ratings listed above. These ratings apply to cards which derive their power from the EQUITY II internal supply as opposed to cards which derive their power from external sources.

The following table shows the typical power consumption of the 8087 co-processor.

8087 MATH CO-PROCESSOR CURRENT CONSUMPTION (Typical)

NAME	+5V	+12V	-5V	-12V
8087 Co-Processor	310 mA.	0 mA.	0 mA.	0 mA.

IMPORTANT: DO NOT PROCEED WITH INSTALLATION OF THE TOPVIEW BOARD UNTIL READING THIS SUPPLEMENT.

MCY-TV BOARD INSTALLATION GUIDE SUPPLEMENT

OVERVIEW

The Topview Insulator is required when installing the Topview Board in the Equity II to provide an insulation between the Equity II Base Plate and the Topview Board. This installation procedure supplement is step 8.5 of the MCY-TV Board Installation Guide.

INSTALLATION PROCEDURE

1. First complete the MCY-TV Board Installation Procedures 1 thru 8 (step #8 is: Connect the MCY-TV Board to the main circuit board in the place vacated by the option slot board).
2. Place the Topview Insulator on the base plate above the Lithuium Battery by setting the three round holes over the three plastic stand-offs and the square hole over the dummy plastic plate (refer to figure 1 below).

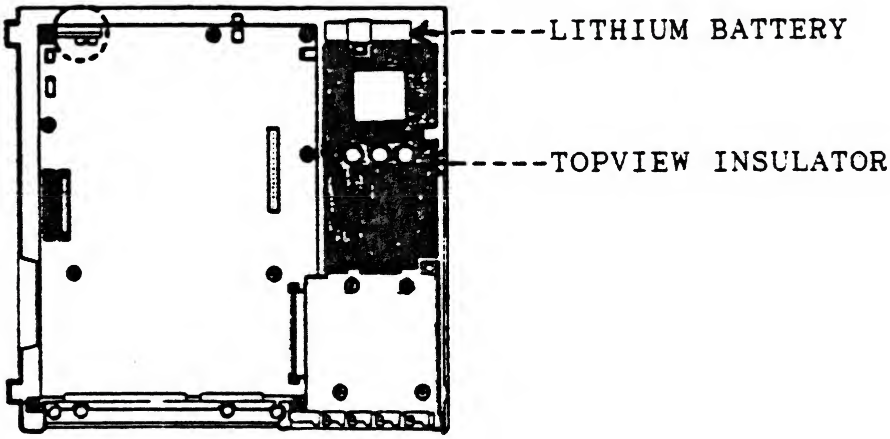

Figure 1

3. Proceed with MCY-TV Board Installation Procedures 9 thru 15.

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TECHNICAL INFORMATION BULLETIN

T I B NO. : EQII-002
DATE : 05/09/86
PAGE (s) : 1 of 2
SUBMITTED BY: Sid Arzu
AUTHORIZED BY :

MACHINE (s) : EQUITY I and II

REFERENCE : SB Q-090

TITLE: EQUITY HDD AND HDC COMPATIBILITY

APPLICABILITY

All EQUITY I and II Personal Computers.

ACTION REQUIRED

To ensure compatibility, all Hard Disk Drives installed in the EQUITYs must be formatted with the corresponding version of the Hard Disk Controller ROM BIOS it will be operated with. Therefore, when the Hard Disk Drive Controller ROM BIOS version 62-000062-010 is replaced with version 62-000062-010-1, the HDD must be reformatted.

PART NUMBER REFERENCE

Part Number	Description
Y144505001	HDC ROM BIOS Version 62-000062-010-1
Y144513000	HDC (NCL) NDC5027-49
T860050200	HDD HD-860
Y147504000	HDD DK505-2

ATTACHMENT

HDD and HDC interchangeability chart.

HDD And HDC Interchangeability Chart for EQUITY I/II

EQUITY I

Hard Disk Controller	ROM BIOS	Hard Disk Drive
WD10025-WX2C027	Ver. 62-000062-010	HD-860-501-00
" "	" "	HD-860-502-00
" "	" "	HD-860-503-00
" "	" "	HD-860-505-00
WD10025-WX2C027	Ver. 62-000062-010-1	HD-860-501-00
" "	" "	HD-860-502-00
" "	" "	HD-860-503-00
" "	" "	HD-860-505-00
NDC5027-49 (NCL)	N/A	Hitachi DK505-2

EQUITY II

Hard Disk Controller	ROM BIOS	Hard Disk Drive
WD10025-WX2C027	Ver. 62-000062-010-1	HD-860-501-00
" "	" "	HD-860-502-00
" "	" "	HD-860-503-00
" "	" "	HD-860-505-00

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TECHNICAL INFORMATION BULLETIN

T I B NO. : EQUITYII-003
DATE : 06/10/86
PAGE (s) : 1 of 1
SUBMITTED BY: Sid Arzu Sid
AUTHORIZED BY :

MACHINE (s) : EQUITY I & II
REFERENCE : NONE

TITLE: EQUITY I / II COMPUTER OPERATION ON 220VAC, 50Hz

The Equity computer 110VAC power supply may not be converted to operate on 220VAC because it would violate U.S. and Foreign Government safety regulations and void the warranty. Units requiring 220VAC power supplies must be purchased in those countries where available.

If an Equity I or II computer is purchased in the U.S. and must be used in a foreign country where only 220VAC is available, a step-down power transformer may be used to provide 110VAC. Equity I and II computers will operate normally on either 50 or 60Hz. The user must confirm that the step-down transformer power rating is sufficient to operate the system to which it is connected. This can be done by calculating the appropriate wattage in accordance to the power requirements indicated on the product label located on the Equity rear panel.

For units purchased in the U.S. and used overseas, warranty repair service will only be provided if the complete unit is returned with appropriate proof of purchase to an Authorized Epson Service facility in the U.S.A.

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TECHNICAL INFORMATION BULLETIN

T I B NO.: EQUITYII-004
DATE: 06/10/86
PAGE (s): 1 of 1
SUBMITTED BY: Sid Arzu
AUTHORIZED BY:

MACHINE (s): EQUITY II & III

REFERENCE: NONE

TITLE: INSTALLATION OF THE EQUITY II/III SECOND FDD

The information provided in this bulletin is a supplement to the installation instructions provided in the Equity II/III 2nd Floppy Disk Drive Set.

1. Before installing a 2nd SD-521 (360K) or SD-581L (1.2MB) in the Equity, the jumper installed on location DS0 of jumper block SSI on the FDD Main Circuit Board must be set to location DS1 (Drive Select 1, being drive B).

2. If the 2nd FDD to be installed is a Canon MDD-531, the jumper installed at location S1 on jumper block JJ1 on the MDD Main Circuit Board must be set to location S2 (Select 2, being drive B).

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TECHNICAL INFORMATION BULLETIN

T I B NO.: EQI-010
EQII-005
DATE: 07-29-86
PAGE (s): 1 of 1
SUBMITTED BY: Sid Arzu
AUTHORIZED BY:

MACHINE (s): EQUITY I & II
REFERENCE: SI No. 86-040

TITLE: EQUITY HDD PHYSICAL FORMAT AND BADTRACK PROGRAM

The Equity I and II HDD Physical Format and Badtrack Program (SPHDD.BAT) is consists of the following:

1. FMT.EXE, the format program which identifies whether a Western Digital or a National Computer Ltd HDC is being used.
2. BADTRACK.EXE, the badtrack entry/format program.
3. HDDPC.EXE, the read/write check program that certifies badtrack data.
4. SHIPDISK.COM, the program that moves the read/write heads to the shipping zone.

The SPHDD.BAT program is to be used when servicing the HDD since it is capable of recovering the format of a bad sector ID, and also allows interlace operation of HDD,s previously formatted with either a Western Digital or National Computer Ltd HDC.

The SPHDD.BAT Program is to be used in an Equity I or II configured with Hard Disk Drive and either a Western Digital or Nat'l Comp. Ltd Hard Disk Controller. The program is automatically executed beginning with physical format. When the badtrack.exe program is executed, a display requesting number of bad track following bad cylinder and head number are displayed. Badtrack data is usually indicated on top of the sealed unit of the HDD.

The attached document is a reference to the program sequence of operation.

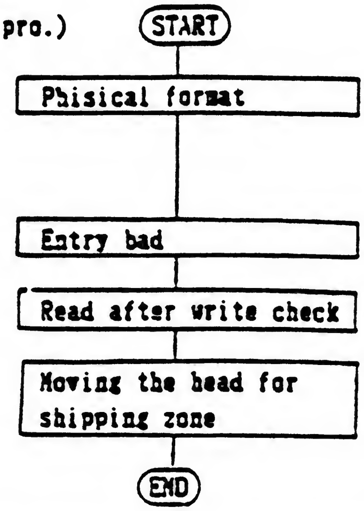
Attachment/

EQUITY I, II/EPSON PC, PC+ HDD PHISICAL FORMAT AND ENTRY BADTRACK PROGRAM OPERATION MANUAL

ENGINEERING SERVICE SECTION

1 OUTLINE OF THE PROGRAM

This program (SPHDD.BAT) performs the following operation.



[COMMAND NAME]	[DESCRIPTION]
SPHDD.BAT(Main pro.)	
FMT.EXE	FMT.EXE distinguishs between Western digital's HDC and National computer ltd's HDC. Then it performs the phisical format using BIOS CALL.
BADTRACK.EXE	BADTRACK.EXE formats the badtrack information input by a operator to HDD.
HDDPC.EXE	HDDPC.EXE verifies the entry badtrack.
SHIPDISK.COM	SHIPDISK.COM moves head for shipping zone.

Different between HDFMTALL (A utility for north America only) and this program

HDFMTALL is a phisical format program for end-user. It has some following problem on repair a HDD.

HDFMTALL has auto entry bad function, it's no need an entry badtrack operation.

=== PROBLEM ON HDD SERVICE WITH HDFMTALL ===

	HDFMTALL	ENTRY BADTRACK PRO.
There are some defect on ID of a sector.	ERROR (Can't format)	POSSIBLE FORMAT (Recover format)
It's first time to format a HDD or change the maker of a HDC.	First format: HDFMTALL executes format as all tracks are badtrack. Change HDC: Inter leave is different.	NO PROBLEM

2 OPERATION

*** CAUTION ***

When operating, do not take out the floppy disk.

2—1. GETTING START

(1) Install the HDC(Western digital or National computer) for option slot of the EQUITY I,II / EPSON PC,PC+.

(2) Connect the cables between HDC and HDD, and turn the power switch on.

(3) Set the program diskette for A drive, then program starts automatically.

2—2. PHISICAL FORMAT (FMT.EXE)

After getting started, phisical format starts automatically.

Normal ending

The screen displays :

——— PHISICAL FORMAT COMPLETE.

2—3. ENTRY BADTRACK (BADTRACK.EXE)

After phisical format, BADTRACK.EXE starts automatically.

Number of bad

0 to 40

Bad cylinder

1 to 614

Head no.

0 to 5

Entry bad again

At the following display, input "s" key.

```
Press G then go formatting.
Press S then enter them from start again.
Press X then exit.
```

→ Normally, input "G" key.

2—4. READ AFTER WRITE CHECK (HDDPC.EXE)

After entry badtrack, HDDPC.EXE starts automatically.

At first, HDDPC.EXE performs random read after write check several times, next, it performs sequential read check all tracks of the HDD one time.

→ HDDPC.EXE is multi-sector mode in sequential check, thus, the screen displays only "01" with current sector.

2—5. MOVING THE HEAD FOR SHIPPING ZONE (SHIPDISK.COM)

After read after write check, SHIPDISK.COM starts automatically.

When screen displays "Please power down", turn the power switch off.

3 ERROR INDICATION

3—1. IN PHISICAL FORMATTING

(1) HDD PROBLEM

a. Using a NCL's HDC (NDC5027-49) ················The screen displays "RECOVER FORMAT START!", then it starts format as track format. (Track format spends timed two time.)

b. Using a W.D.'s HDC (WD10025-WX2C027) ················The screen displays:

Push SPACE key·········Recover format
Push ENTER key·········END of format

Recover format (Track format) spends about 2-hours cause the RECALIBLATION each track.

(2) HDC PROBLEM

The screen displays:

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TECHNICAL INFORMATION BULLETIN

T I B NO.: EQII-006
DATE: 09/24/86
PAGE (s): 1 of 3
SUBMITTED BY: Sid Arzu
AUTHORIZED BY:

MACHINE (s): EQUITY II
REFERENCE: ES 86 - 0079A

TITLE: ADDITION OF INSULATING SHEET KIT TO OPTIONAL Q910 FDD SET

DATE OF CHANGE

Insulating sheet kit has been included in optional Canon floppy disk drive set (Q910), since July 1986 production.

APPLICABILITY

All Equity II computers with Canon FDD (MDD-531-31) installed in the lower drive position.

DESCRIPTION

When an optional MDD-531-31 is installed in the Equity II lower drive position, disk read errors may occur intermittently due to electrical interference from the system power supply.

ACTION REQUIRED

Install an insulating sheet in the Equity II to eliminate the possibility of disk read errors, (refer to attached installation instructions). This should be done on an as needed basis.

PARTS REQUIRED

DESCRIPTION	PART NUMBER
FDD shield plate	Y147020001
Nylon rivet	X510480020

PRODUCT CODE LABEL CHANGE

The optional FDD product code has been changed as follows:

DESCRIPTION	PRODUCT CODE
FDD kit without insulation	Q910 Y149010000
FDD kit with insulation	Q910 Y149010001

ADDENDUM1 S/I ES 86-0079A

Insulating Sheet Installation Guide

Package contents

Insulating sheet	1
Nylon rivets.....................	2 sets

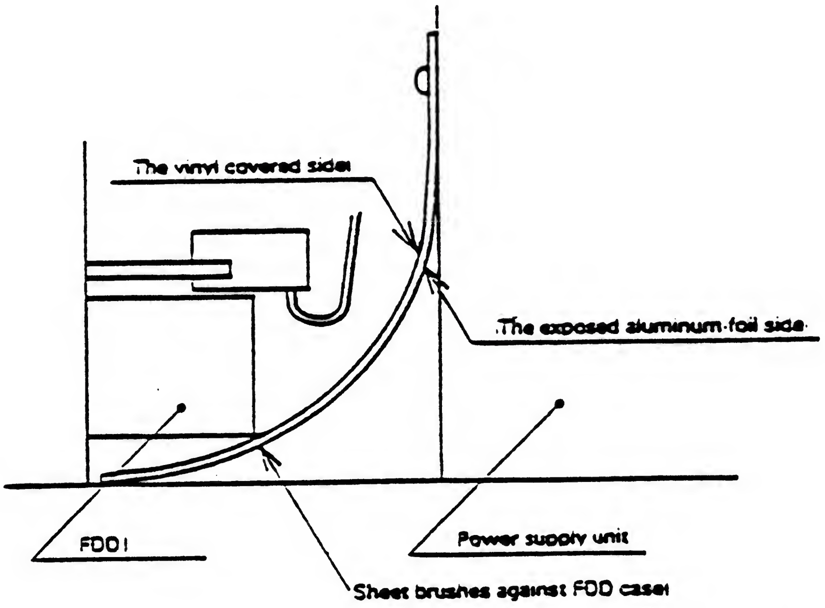
Overview

This insulating sheet should be attached to the power supply of the Equity II before installing an optional 360 Kbyte drive. You do not need to install this sheet in an Equity III. The sheet is designed to provide extra protection against data loss due to electrical noise interference.

Installation procedure

Follow the steps in the order given:

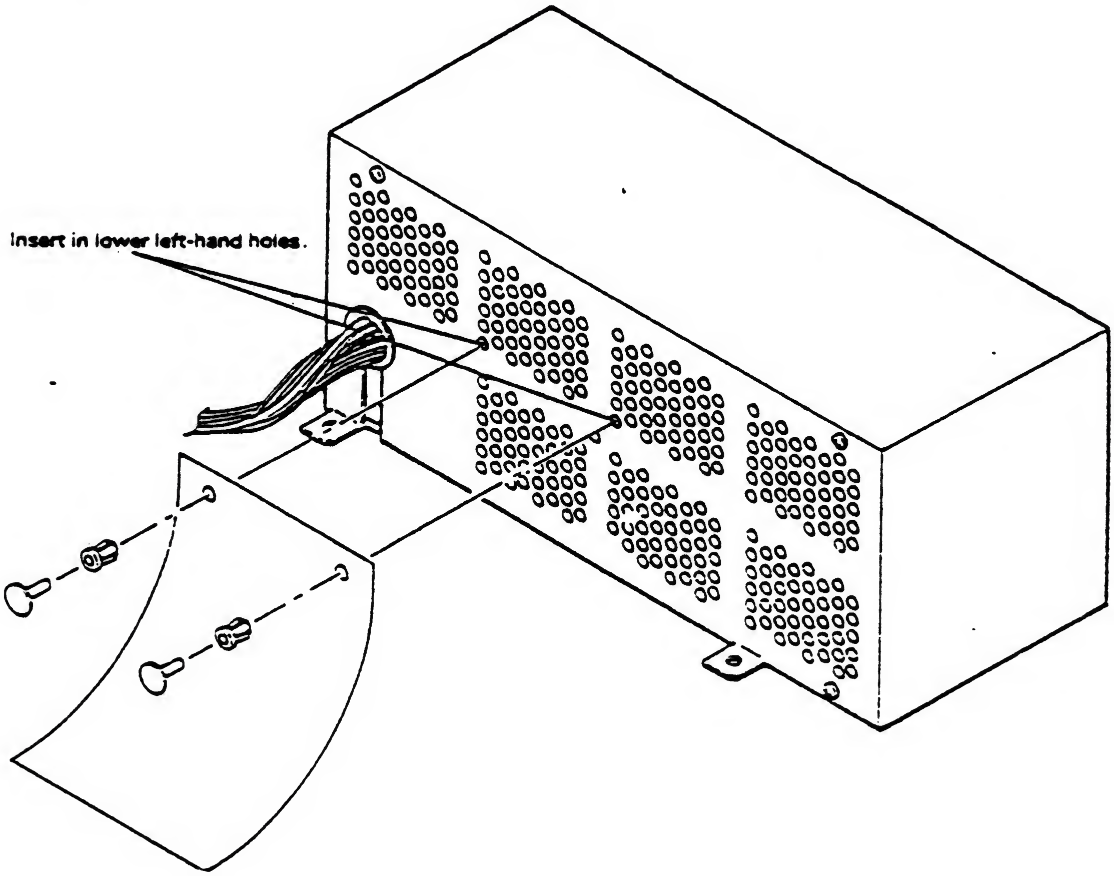
1. Slide the top drive forward to provide more working space. To do this, remove the two screws on the right side of the case and gently push the drive forward from the back. If necessary, you can also remove the connector cable to make more space.
2. To provide maximum protection, the insulating sheet has been designed to curve under the floppy-drive case as shown in the diagram below. Since the sheet is flat, wrap it around a bottle to give it a curved shape.


The vinyl covered side
The exposed aluminum foil side
FDD1
Power supply unit
Sheet brushes against FDD case

Important: The exposed aluminum foil side must face the power supply, and the vinyl covered side must face the floppy drive unit.

Y14999100800

3. Take the two nylon rivet sets and remove the rivets from their sockets.
4. Place the two sockets in the holes at the top of the insulating sheet. Holding the sockets in place with your thumbs, slide the sheet into place and insert the sockets in the two holes in the power supply case shown in the diagram below.



Insert in lower left-hand holes.

5. Lock the sheet in place by inserting the rivets into their sockets.
6. Proceed with the 360 Kbyte floppy-drive installation. When you are finished, make sure that the connector cables are clear of the insulating sheet.
7. Slide the top drive back into place and fasten it to the case with the two screws removed in step 1.

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TECHNICAL INFORMATION BULLETIN

TIB NO.: HD860-002
DATE: 9/28/87
PAGE (s): 1 of 1
SUBMITTED BY: Bob Merchant
AUTHORIZED BY:

MACHINE (s): HD-860

REFERENCE: N/A

TITLE: EPSON HD-860 HARD DISK DRIVE WARRANTY EXTENSION

The purpose of this bulletin is to inform you of a change in the warranty period for the HD-860 hard disk drive unit.

Epson America, Inc. has made the decision to extend the warranty period for the HD-860 hard disk drive, installed in the Equity product line, for an indefinite period. This warranty extension will cover all HD-860 hard disk drives regardless of the purchase date. Standard warranty claim procedures are to be followed for these failures. The normal warranty labor reimbursement and no charge parts exchange will be given for these claims.

This warranty claim extension is for HD-860 failures only and Epson America, Inc. reserves the right to cancel this HD-860 warranty extension at any time. It is designed to promote the satisfaction of our mutually inclusive customer base with Epson products.

Epson Service Department is currently providing HMD-720 hard disk drive units as warranty replacements for returned HD-860's. Authorized Service Centers and Customer Care Centers should not use HD-860's as repair replacements. Any ASC or CCC having HD-860's in repair float stock may exchange these for HMD-720's by contacting Warranty Administration for an RMA.

Note: This exchange does not apply to sales product, and is contingent upon availability of Epson's float exchange stock.

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TECHNICAL INFORMATION BULLETIN

T I B NO.: EQI+-001
DATE: 3/8/88
PAGE (s): 1 of 1
SUBMITTED BY: Robert Merchan
AUTHORIZED BY: Larry J. Holzapple

MACHINE (s): EQUITY I/II/I+

REFERENCE: ES-88-024

TITLE: WD1002A-WX1 HARD DISK CONTROLLER MANUFACTURING CHANGE

The purpose of this bulletin is to provide information on a change in the design of the WD1002A-WX1 hard disk controller card used with the Equity I, Equity II and Equity I+.

Note: No functions are changed by this modification.

MODIFICATION:

The following chart describes the modifications made to the Hard Disk Controller card:

Description of Change		
Component	**From**	**To**
Data Separator	(U101) WD10C20A	WD10C20B
Capacitor	C109	Not installed
Delay Line	U102	Not installed
Coil	L103	Not installed

REASON:

Cost reduction

DATE OF CHANGE:

From the end of 1987

INTERCHANGEABILITY:

New and old style hard disk controller boards are both upward and downward compatible.

EQUITY II MCY BOARD HISTORY

MCY Board P/N (Revision)	Y147206000(01) Latest Rev.	Y147205000(01)	Y147205000(00)	Y147201000(02)	Y147201000(01)	Y147201000(00) Earliest Rev.
Starting Serial Number	040001	29875	Unknown	Unknown	Unknown	Unknown
Non-Epson keyboard support	Yes	Yes	Yes	No	No	No
Option slot RAM refresh mode jumper selectable	Yes	Yes	Yes	Yes	Yes	No
640K RAM installed on MCY (main) board	Yes	Yes	Yes	No	No	No
Serial Interface port functions over 1200 baud	Yes	No	No	Yes	No	No
8087 Math Coprocessor Support	Yes	Yes	Yes	Yes	Yes	No
Concurrent operation of 8087 and optional third party dynamic RAM boards	Yes	No	No	Yes	No	No
Topview fix incorporated on MCY (main) board	Yes	No	No	Yes	No	No

PRODUCT SUPPORT BULLETIN

PSB NO.: S-0028A	**DATE:** 6/29/88	**PAGE:** 1 of 1

SUBJECT: EPSON 3.5" 720KB FLOPPY DISK DRIVE COMPATIBILITY

The purpose of this bulletin is to provide information regarding the compatibility of the Epson 3.5", 720KB floppy disk drive (Product Code A112A-AA) with the Apex and Equity series computers.

The 3.5" floppy disk drive must be used with MS-DOS 3.2 or higher.

Please refer to the following table for compatibility information.

Apex	No special setup required
Equity I	Not supported
Equity II	Must include DRIVPARM = /D:1 /F:2 in CONFIG.SYS
Equity III	Not supported*
Equity I+	No special setup required
Equity II+	No special setup required
Equity III+	No special setup required

The Epson 3.5" floppy disk drive is not compatible with the Equity I or the Equity III.

* Manzana Microsystems Inc. offers a 3.5", 720KB floppy disk drive which is compatible with the Equity III computer when used with their 3FIVE device driver.

Refer to Product Support Bulletin # S-0027A for detailed information on using the DRIVPARM command to configure Equity II systems for using the 3.5" floppy disk drive.

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PRODUCT SUPPORT BULLETIN

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SUBJECT: EQUITY II WITH THE EPSON 3.5" FLOPPY DRIVE

The Equity II has been tested with the Epson 3.5" floppy disk drive (A112A-AA). The purpose of this bulletin is to detail the proper procedure for installation and configuration.

1. The Equity must be upgraded to MS-DOS 3.2 (Q395A-AA).

2. The appropriate DRIVPARM command must be added to the CONFIG.SYS file. This defines the correct parameters for block devices (such as disk drives) under MS-DOS. While there are a number of switches to the DRIVPARM command, only two concern us: the logical drive number and the form factor index. For example, to set up the drive as B, add the line:

   ```
   DRIVPARM = /D:1 /F:2
   ```

   to the CONFIG.SYS file. This establishes it as the second logical drive with a 720KB form factor index. The /D: value should be 0 for drive A.

3. The drive must be physically selected, as well. You will find a shorting block designated SS1 on the drive. If installed as A, the jumper should be installed on D0. For drive B, install it on D1.

4. For drive A, use the cable from connector CN9 on the main board. For B, use CN10.

For more information on the DRIVPARM command, please refer to the chapter "Configuring Your System" in the MS-DOS 3.2 manual.

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PRODUCT SUPPORT BULLETIN

PSB NO.: S-0057	**DATE:** 7/29/88	**PAGE:** 1 of 2

SUBJECT: EQUITY II MCY BOARD REVISION LEVELS

The purpose of this bulletin is to provide information on the various revision levels of the Equity II MCY board.

The attached table describes the differences found in the revisions of Equity II MCY boards since its introduction, beginning with the earliest revision Y147201000 (00) to the latest revision Y147206000 (01).

Note: The Y147201000 (02) MCY board is an update of the (01) version with many improvements of the latest MCY board.

Some of the major differences between the earlier versions which were improved in the latest versions are:

* Third party IBM compatible keyboard support - The early revision boards did not have jumpers to select non-Epson keyboards.

* Optional RAM board support - The earliest revision MCY board did not support optional RAM boards (no dynamic memory refresh).

* 640KB RAM on MCY board - The early revision boards only had 512KB RAM installed on the MCY board and required a 128KB RAM board (MCY-RM) which plugged into the MCY board. The later boards have 640KB installed on the MCY board.

* Serial interface - On the earlier boards, the built-in serial port would not operate reliably above 1200 baud. An optional serial interface board could be used however.

* 8087 support - The earliest board would not support it.

* Concurrent operation of 8087 with optional dynamic RAM boards - The earlier MCY boards did not support concurrent operation of 8087 and memory expansion boards or EGA boards with dynamic RAM. An improvement was made to the design in the latest revision board which allowed both to operate together.

* Topview Board - Earlier MCY boards did not support IBM's Topview so a special MCY-TV board was developed to take the place of the MCY-MT board which allowed Topview to function. The latest MCY board operates properly with Topview.